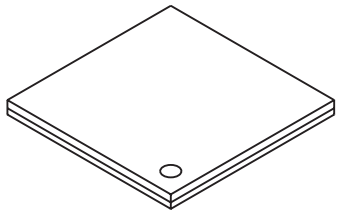
SONY

CXR704060

CMOS 32-bit Single Chip Microcomputer

208 pin TFLGA (Plastic)



Description

The CXR704060 is a CMOS 32-bit microcomputer integrating on a single chip a micro processor unit having a 32-bit RISC CPU as its core, and a signal processing block having an accelerator circuit suited for arithmetic signal processing. Adoption of this arithmetic signal processing accelerator circuit enables flexible support of various signal processing systems.

The microcomputer block incorporates Memory Stick interface, a MagicGate, FLASH memory interface, USB interface, D/A converter for audio applications, A/D converter, serial interface, I^2C bus interface, timer and PWM pulse generator as well as basic configurations like a 32-bit RISC CPU, ROM, RAM, and I/O ports. It also provides the idle/sleep/stop functions that enable lower power consumption.

Features

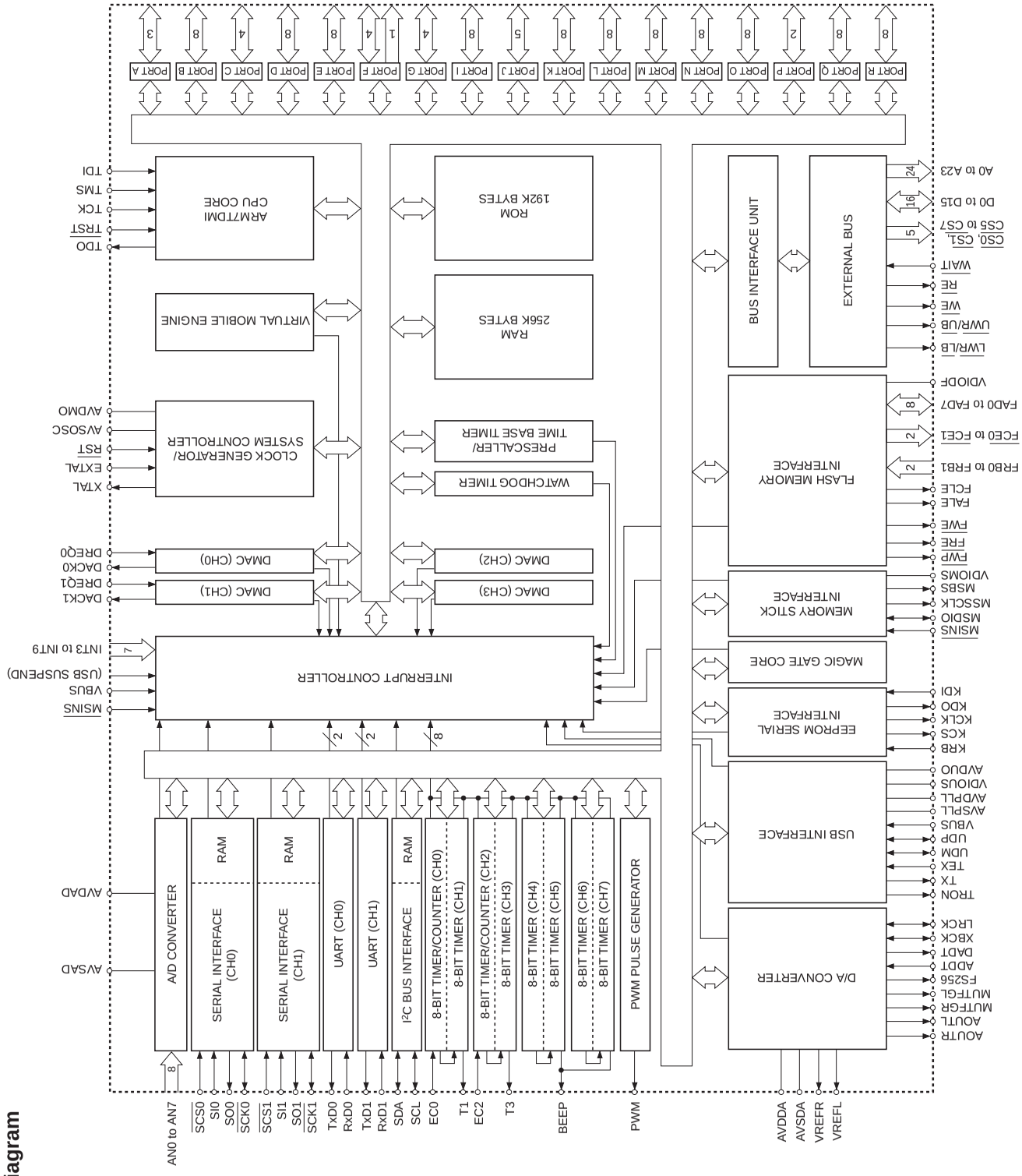
• CPU	SR11 series 32-bit RISC CPU core (ARM7TDMI)
• Minimum instruction cycle	44.29ns (f_{SRC}: 22.5792MHz)
• Incorporated ROM	192K bytes
• Incorporated RAM	256K bytes
• Peripheral hardware	
— Bus interface unit	16-bit data bus, 24-bit address bus, 5 chip select outputs
— DMA controller	4 channels
— A/D converter	10-bit 8-analog input, successive approximation method
— Serial interface	Clock synchronization, 1 channel (Incorporated 128-byte buffer RAM) Clock synchronization, 1 channel (Incorporated 32-byte buffer RAM) Asynchronization, 2 channels
— 8-bit timer	8 channels (timer output)
— Time-base timer	
— Prescaler	
— Watchdog timer	16 bits × 1 channel
— PWM pulse generator	8 bits × 1 channel
— 16-bit D/A converter for audio applications	L channel, R channel
— Memory Stick interface	1 channel
— MagicGate	
— Serial interface for EEPROM	Serial interface for CXK2000, 1 channel
— USB interface	Conforms to USB1.1, internal transceiver
— Flash memory interface	1-bit error correction function
— External interruption	10 channels (polarity selection and both edge detection possible)
• Accelerator for arithmetic signal processing	
• Standby mode	Idle/sleep/stop
• Package	208-pin plastic TFLGA

Structure

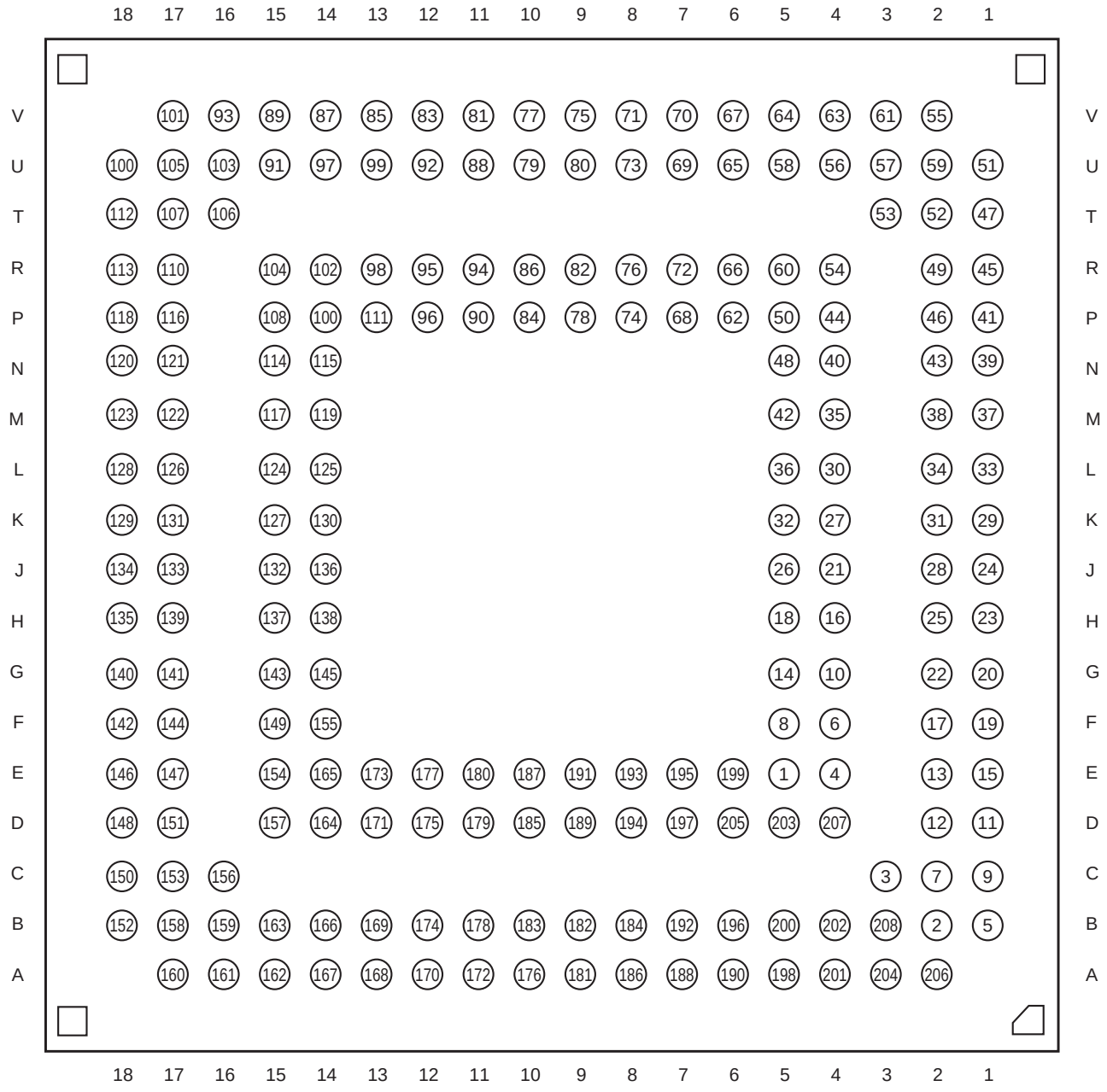
Silicon gate CMOS IC

E02655-PS

Block Diagram



Pin Assignment (Top View) 208-pin TFLGA package



• **Pin Assignment Table**

Pin No.	Pin position	Pin function	Pin No.	Pin position	Pin function	Pin No.	Pin position	Pin function
1	E5	VDIO0	37	M1	VDIO1	73	U8	PE4/$\overline{\text{SCK1}}$
2	B2	PM4/A12	38	M2	PO0/D0	74	P8	PE5/SO1
3	C3	PM5/A13	39	N1	PO1/D1	75	V9	PE6/SI1
4	E4	PM6/A14	40	N4	PO2/D2	76	R8	PE7/$\overline{\text{SCS1}}$
5	B1	PM7/A15	41	P1	PO3/D3	77	V10	TEST5
6	F4	PN0/A16	42	M5	PO4/D4	78	P9	$DV_{DD}1$
7	C2	PN1/A17	43	N2	PO5/D5	79	U10	$DV_{SS}3$
8	F5	PN2/A18	44	P4	PO6/D6	80	U9	VDIO3
9	C1	PN3/A19	45	R1	PO7/D7	81	V11	PF0/EC0/INT3
10	G4	PN4/A20	46	P2	PB0/D8	82	R9	PF1/T1
11	D1	PN5/A21	47	T1	PB1/D9	83	V12	PF2/EC2/INT4
12	D2	PN6/A22	48	N5	PB2/D10	84	P10	PF3/T3
13	E2	PN7/A23	49	R2	PB3/D11	85	V13	PF4/BEEP
14	G5	$DV_{SS}7$	50	P5	PB4/D12	86	R10	PG0/DACK0
15	E1	FAD0	51	U1	PB5/D13	87	V14	PG1/DREQ0/INT5
16	H4	FAD1	52	T2	PB6/D14	88	U11	PG2/DACK1/INT6
17	F2	FAD2	53	T3	PB7/D15	89	V15	PG3/DREQ1/INT7
18	H5	FAD3	54	R4	PA0/PWM	90	P11	TEST2
19	F1	FAD4	55	V2	PA1/SDA	91	U15	TEST3
20	G1	FAD5	56	U4	PA2/SCL	92	U12	TEST0
21	J4	FAD6	57	U3	PC0/$\overline{\text{SCK0}}$	93	V16	TEST1
22	G2	FAD7	58	U5	PC1/SO0	94	R11	TEST6
23	H1	FCLE	59	U2	PC2/SI0	95	R12	EVA
24	J1	FALE	60	R5	PC3/$\overline{\text{SCS0}}$	96	P12	AVSAD
25	H2	VDIODF	61	V3	$DV_{SS}2$	97	U14	AVDAD
26	J5	$\overline{\text{FWE}}$	62	P6	VDIO2	98	R13	AN0
27	K4	$\overline{\text{FRE}}$	63	V4	KDI	99	U13	AN1
28	J2	$\overline{\text{FWP}}$	64	V5	KRB	100	P14	AN2
29	K1	$\overline{\text{FCE0}}$	65	U6	KCLK	101	V17	AN3
30	L4	FRB0	66	R6	KCS	102	R14	AN4
31	K2	$\overline{\text{FCE1}}$	67	V6	KDO	103	U16	AN5
32	K5	FRB1	68	P7	TEST4	104	R15	AN6/INT8
33	L1	PP0	69	U7	PE0/TxD0	105	U17	AN7/INT9
34	L2	PP1	70	V7	PE1/RxD0	106	T16	$\overline{\text{RST}}$
35	M4	$DV_{DD}0$	71	V8	PE2/TxD1	107	T17	$\overline{\text{RAMBK}}$
36	L5	$DV_{SS}1$	72	R7	PE3/RxD1	108	P15	VDBK

Pin No.	Pin position	Pin function	Pin No.	Pin position	Pin function	Pin No.	Pin position	Pin function
109	U18	TDI	143	G15	AVDUO	177	E12	PI6/MUTFGR
110	R17	TMS	144	F17	AVSPLL	178	B11	$DV_{DD}3$
111	P13	TCK	145	G14	AVDPLL	179	D11	$DV_{SS}5$
112	T18	$\overline{TRST}$	146	E18	PQ0	180	E11	VDIO5
113	R18	TDO	147	E17	PQ1	181	A9	PJ0/$\overline{WAIT}$
114	N15	VDIOJT	148	D18	PQ2	182	B9	PJ1/$\overline{RE}$
115	N14	$DV_{DD}2$	149	F15	PQ3	183	B10	PJ2/$\overline{LWR}$/$\overline{LB}$
116	P17	$DV_{SS}4$	150	C18	PQ4	184	B8	PJ3/$\overline{UWR}$/$\overline{UB}$
117	M15	VDIO4	151	D17	PQ5	185	D10	PJ4/$\overline{WE}$
118	P18	PD0/CONNECT	152	B18	PQ6	186	A8	PK0/$\overline{CS0}$
119	M14	PD1/XVDATA	153	C17	PQ7	187	E10	PK1/$\overline{CS1}$
120	N18	PD2/DPLS	154	E15	$DV_{SS}8$	188	A7	PK2
121	N17	PD3/DMNS	155	F14	VDIO7	189	D9	PK3
122	M17	PD4/TXDPLS	156	C16	PR0	190	A6	PK4
123	M18	PD5/TXDMNS	157	D15	PR1	191	E9	PK5/$\overline{CS5}$
124	L15	PD6/TXENL	158	B17	PR2	192	B7	PK6/$\overline{CS6}$
125	L14	PD7/SUSPEND	159	B16	PR3	193	E8	PK7/$\overline{CS7}$
126	L17	VBUS	160	A17	PR4	194	D8	$DV_{SS}6$
127	K15	VDIOUS	161	A16	PR5	195	E7	VDIO6
128	L18	UDM	162	A15	PR6	196	B6	PL0/A0
129	K18	UDP	163	B15	PR7	197	D7	PL1/A1
130	K14	TRON	164	D14	$DV_{SS}9$	198	A5	PL2/A2
131	K17	AVSDA	165	E14	VDIOMS	199	E6	PL3/A3
132	J15	VREFR	166	B14	MSDIO	200	B5	PL4/A4
133	J17	AOUTR	167	A14	MSBS	201	A4	PL5/A5
134	J18	AOUTL	168	A13	MSSCLK	202	B4	PL6/A6
135	H18	VREFL	169	B13	$\overline{MSINS}$	203	D5	PL7/A7
136	J14	AVDDA	170	A12	PI7	204	A3	PM0/A8
137	H15	XTAL	171	D13	PI0/DADT	205	D6	PM1/A9
138	H14	EXTAL	172	A11	PI1/ADDT	206	A2	PM2/A10
139	H17	AVDMO	173	E13	PI2/LRCK	207	D4	PM3/A11
140	G18	AVSOSC	174	B12	PI3/XBCK	208	B3	$DV_{SS}0$
141	G17	TX	175	D12	PI4/FS2S6			
142	F18	TEX	176	A10	PI5/MUTFGL			

Pin Functions

Symbol	I/O	Function			I/O power supply
PJ0/$\overline{WAIT}$	I/O / Input	(Port J) 5-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (5 pins)	Wait input for external bus.		VDIO0 VDIO5 VDIO6
PJ1/$\overline{RE}$	I/O / Output		Read signal output for external bus.		
PJ2/$\overline{LWR}$/$\overline{LB}$	I/O / Output / Output		Write strobe signal output for D0 to D7.	Strobe signal output indicates access to D0 to D7.	
PJ3/$\overline{UWR}$/$\overline{UB}$	I/O / Output / Output		Write strobe signal output for D8 to D15.	Strobe signal output indicates access to D8 to D15.	
PJ4/$\overline{WE}$	I/O / Output		Write signal output for external bus.		
PK0/$\overline{CS0}$, PK1/$\overline{CS1}$	I/O / Output	(Port K) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)	Chip select output for external bus. (2 pins)		
PK2 to PK4	I/O				
PK5/$\overline{CS5}$ to PK7/$\overline{CS7}$	I/O / Output		Chip select output for external bus. (3 pins)		
PL0/A0 to PL7/A7	I/O / Output	(Port L) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)	Address bus output for external bus. (24 pins)		
PM0/A8 to PM7/A15	I/O / Output	(Port M) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)			
PN0/A16 to PN7/A23	I/O / Output	(Port N) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)			

Symbol	I/O	Function		I/O power supply
FAD0 to FAD7	I/O	Flash memory interface data I/O.		VDIODF
FCLE	Output	CLE output of flash memory interface.		
FALE	Output	ALE output of flash memory interface.		
$\overline{\text{FWE}}$	Output	$\overline{\text{WE}}$ output of flash memory interface.		
$\overline{\text{FRE}}$	Output	$\overline{\text{RE}}$ output of flash memory interface.		
$\overline{\text{FWP}}$	Output	$\overline{\text{WP}}$ output of flash memory interface.		
$\overline{\text{FCE0}}$, $\overline{\text{FCE1}}$	Output	$\overline{\text{CE}}$ output of flash memory interface.		
FRB0, FRB1	Input	RB input of flash memory interface.		
PP0, PP1	I/O	(Port P) 2-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (2 pins)		VDIO1 VDIO2 VDIO3
PO0/D0 to PO7/D7	I/O / I/O	(Port O) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)	Data bus I/O for external bus. (16 pins)	
PB0/D8 to PB7/D15	I/O / I/O	(Port B) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)		
PA0/PWM	I/O / Output	(Port A) 3-bit I/O port. I/O can be specified in 1-bit units. For Bit 0, pull-up resistor can be incorporated through program. (3 pins)	8-bit PWM output.	
PA1/SDA	I/O / I/O		I^2C bus interface data I/O.	
PA2/SCL	I/O / I/O		I^2C bus interface clock I/O.	
PC0/$\overline{\text{SCK0}}$	I/O / I/O	(Port C) 4-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (4 pins)	Serial clock (CH0) I/O.	
PC1/SO0	I/O / Output		Serial data (CH0) output.	
PC2/SI0	I/O / Input		Serial data (CH0) input.	
PC3/$\overline{\text{SCS0}}$	I/O / Input		Serial chip select (CH0) input.	
KDI	Input	Serial interface data input for EEPROM.		
KRB	Input	Serial interface Ready/Busy input for EEPROM.		

Symbol	I/O	Function			I/O power supply
KCLK	Output	Serial interface clock output for EEPROM.			VDIO1 VDIO2 VDIO3
KCS	Output	Serial interface chip select output for EEPROM.			
KDO	Output	Serial interface data output for EEPROM.			
PE0/TxD0	I/O / Output	(Port E) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)	UART (CH0) transmit data output.		
PE1/RxD0	I/O / Input		UART (CH0) receive data input.		
PE2/TxD1	I/O / Output		UART (CH1) transmit data output.		
PE3/RxD1	I/O / Input		UART (CH1) receive data input.		
PE4/$\overline{\text{SCK1}}$	I/O / I/O		Serial clock (CH1) I/O.		
PE5/SO1	I/O / Output		Serial data (CH1) output.		
PE6/SI1	I/O / Input		Serial data (CH1) input.		
PE7/$\overline{\text{SCS1}}$	I/O / Input		Serial chip select (CH1) input.		
PF0/EC0/ INT3	I/O / Input / Input	(Port F) Lower 4 bits are for I/O; upper 1 bit is output-only 5-bit port. For lower 4 bits, I/O can be specified in 1-bit units. For lower 4 bits, pull-up resistor can be incorporated through program in 1-bit. (5 pins)	External event input to 8-bit timer (CH0).	External interruption request input.	
PF1/T1	I/O / Output		8-bit timer (CH1) output.		
PF2/EC2/ INT4	I/O / Input / Input		External event input to 8-bit timer (CH2).	External interruption request input.	
PF3/T3	I/O / Output		8-bit timer (CH3) output.		
PF4/BEEP	Output / Output		Beep output.		
PG0/DACK0	I/O / Output	(Port G) 4-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (4 pins)	Transfer request acknowledge signal output from DMA controller (CH0).		
PG1/DREQ0/ INT5	I/O / Input / Input		Transfer request input to DMA controller (CH0).	External interruption request input.	
PG2/DACK1/ INT6	I/O / Output / Input		Transfer request acknowledge signal output from DMA controller (CH1).	External interruption request input.	
PG3/DREQ1/ INT7	I/O / Input / Input		Transfer request input to DMA controller (CH1).	External interruption request input.	
AN0 to AN5	Input	Analog input to A/D converter. (6 pins)			AVDAD
AN6/INT8, AN7/INT9	Input / Input	Analog input to A/D converter. (2 pins)	External interruption request input. (2 pins)		

Symbol	I/O	Function		I/O power supply
PD0/ CONNECT	I/O / Input	(Port D) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)	USB connection input. (for external USB transceiver)	VDIO4
PD1/XVDATA	I/O / Input		USB receive data input. (for external USB transceiver)	
PD2/DPLS	I/O / Input		USB D+ data input. (for external USB transceiver)	
PD3/DMNS	I/O / Input		USB D– data input. (for external USB transceiver)	
PD4/TXDPLS	I/O / Output		USB D+ data output. (for external USB transceiver)	
PD5/TXDMNS	I/O / Output		USB D– data output. (for external USB transceiver)	
PD6/TXENL	I/O / Output		USB data control output. (for external USB transceiver)	
PD7/ SUSPEND	I/O / Output		USB suspend output. (for external USB transceiver)	
VBUS	Input	USB power signal input. (USB connection detection signal input, for internal USB transceiver)		
UDM	I/O	USB D– data I/O. (for internal USB transceiver)		VDIOUS
UDP	I/O	USB D+ data I/O. (for internal USB transceiver)		
TRON	Output	UDP pull-up resistor connection control output.		
VREFL	Output	Internal DAC reference voltage output. (Lch)		AVDDA
AOUTL	Output	Internal DAC Lch output.		
AOUTR	Output	Internal DAC Rch output.		
VREFR	Output	Internal DAC reference voltage output. (Rch)		
PQ0 to PQ7	I/O	(Port Q) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)		VDIO7
PR0 to PR7	I/O	(Port R) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)		

Symbol	I/O	Function		I/O power supply
PI0/DADT	I/O / Output	(Port I) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor can be incorporated through program in 1-bit units. (8 pins)	Audio data output to external DAC. (for test output)	VDIO0 VDIO5 VDIO6
PI1/ADDT	I/O / Input		Audio data input from external ADC. (for test input)	
PI2/LRCK	I/O / I/O		L/R sampling clock I/O to external DAC/ADC. (44.1kHz)	
PI3/XBCK	I/O / I/O		Bit clock I/O to external DAC/ADC. (2.822MHz)	
PI4/FS256	I/O / Output		256fs clock output. (11.2896MHz)	
PI5/MUTFGL	I/O / Output		Zero data detection signal output. (Lch)	
PI6/MUTFGR	I/O / Output		Zero data detection signal output. (Rch)	
PI7	I/O			VDIOMS
MSDIO	I/O	Memory Stick interface data I/O.		
MSBS	Output	Memory Stick interface bus state output.		
MSSCLK	Output	Memory Stick interface clock output.		
$\overline{\text{MSINS}}$	Input	Memory Stick interface card detection input. (INT0)		
TEST4	Input	Test input.		VDIO1 VDIO2 VDIO3
TEST2, TEST3	Input	Test input.		
TEST0, TEST1	Input	Test input.		
TEST6	Output	Test output.		
EVA	Input	EVA mode switching input.		
TDI	Input	Data input for JTAG boundary scanning test.		VDIOJT
TMS	Input	Test mode control input for JTAG boundary scanning test.		
TCK	Input	Clock input for JTAG boundary scanning test.		
$\overline{\text{TRST}}$	Input	Reset input for JTAG boundary scanning test.		
TDO	Output	Data output for JTAG boundary scanning test.		
EXTAL	Input	Oscillation connector for main oscillation. (When a clock is supplied externally, input it to EXTAL; opposite phase clock should be input to XTAL.)		AVDMO
XTAL	Output			
TEST5	Output	Test output.		VDIO1 VDIO2 VDIO3
TEX	Input	Oscillation connector for sub oscillation. (When a clock is supplied externally, input it to TEX; opposite phase clock should be input to TX.)		AVDUO
TX	Output			
$\overline{\text{RST}}$	Input	System reset input.		AVDAD
$\overline{\text{RAMBK}}$	Input	Control signal input for RAM backup.		

Symbol	I/O	Function	I/O power supply
VDBK		Positive power supply for RAM backup.	
AVDAD		Positive power supply for A/D converter.	
AVSAD		GND for A/D converter.	
AVDDA		Positive power supply for internal DAC.*1	
AVSDA		GND for internal DAC.	
AVDPLL		Positive power supply for PLL.*2	
AVSPLL		GND for PLL.	
AVDMO		Positive power supply for main clock oscillator.*1	
AVDUO		Positive power supply for sub clock oscillator.*2	
AVSOSC		Main clock and sub clock oscillator GND.	
VDIODF		Positive power supply for flash memory interface.	
VDIOMS		Positive power supply for Memory Stick interface.	
VDIOJT		Positive power supply for JTAG.	
VDIOUS		Positive power supply for USB transceiver.	
VDIO0 to VDIO7		I/O interface positive power supply.	
$DV_{DD}0$ to $DV_{DD}3$		Positive power supply. (Connect all four V_{DD} pins to positive power supply.)	
$DV_{SS}0$ to $DV_{SS}9$		GND. (Connect all ten DVss pins to GND.)	

*1 AVDDA and AVDMO must be the same potential.

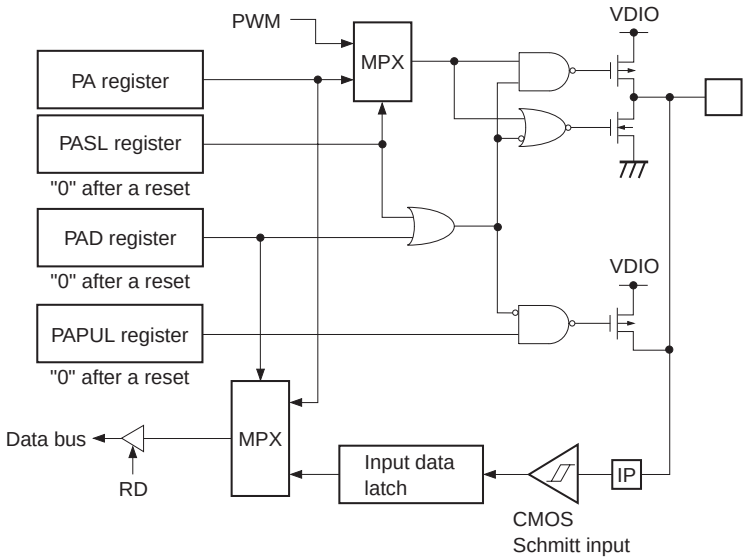
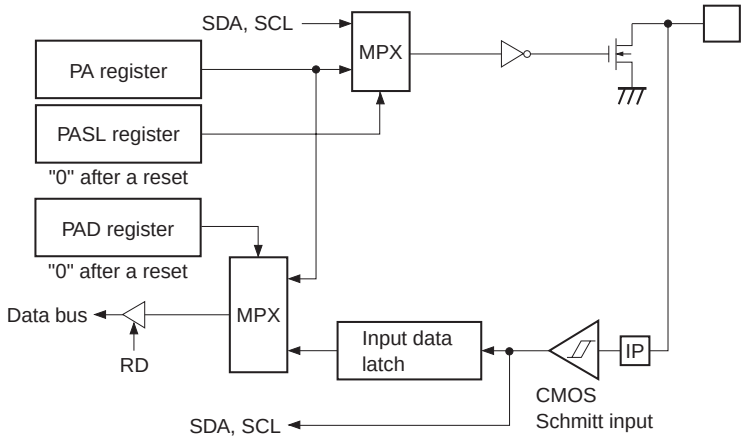
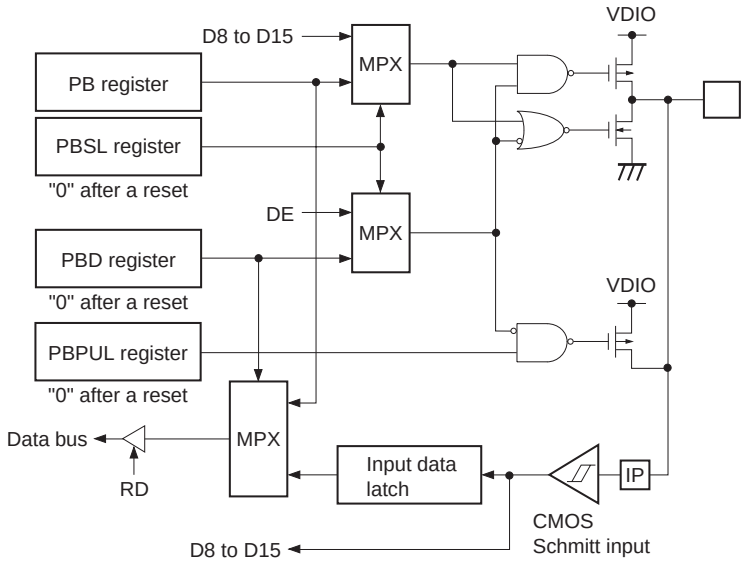
*2 AVDPLL and AVDUO must be the same potential.

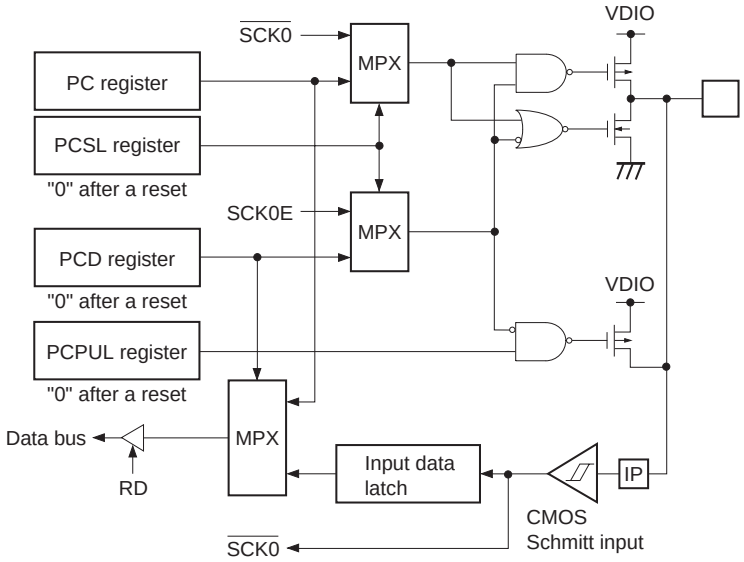
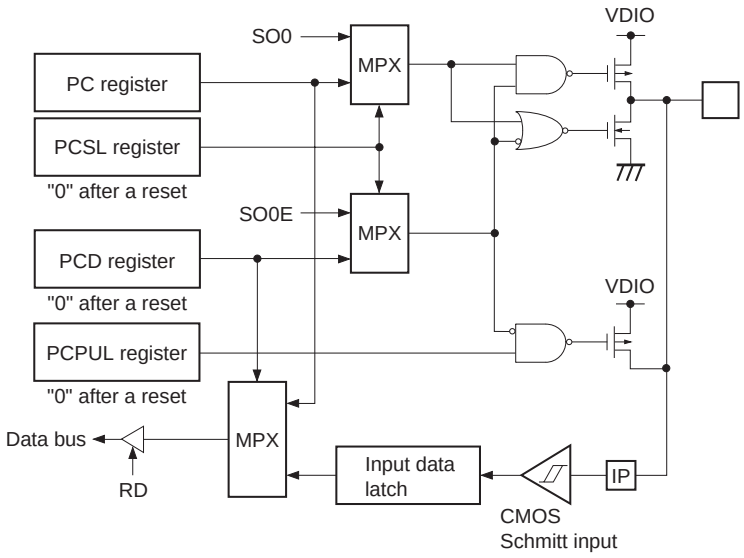
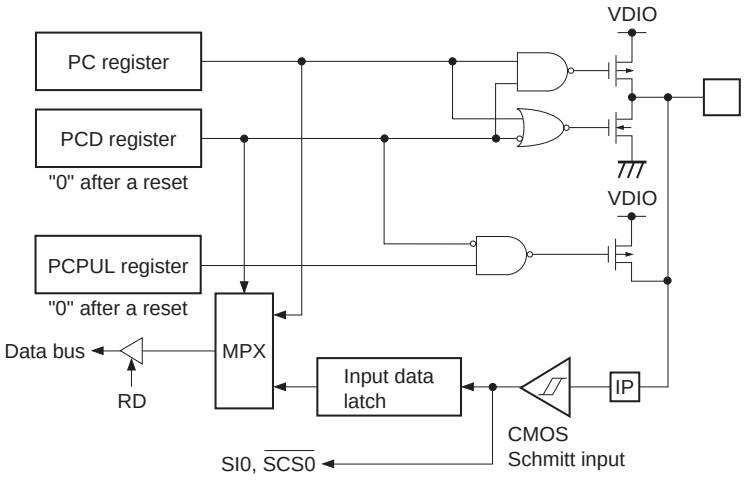
• **I/O Power Supply and Pin Correspondence Table**

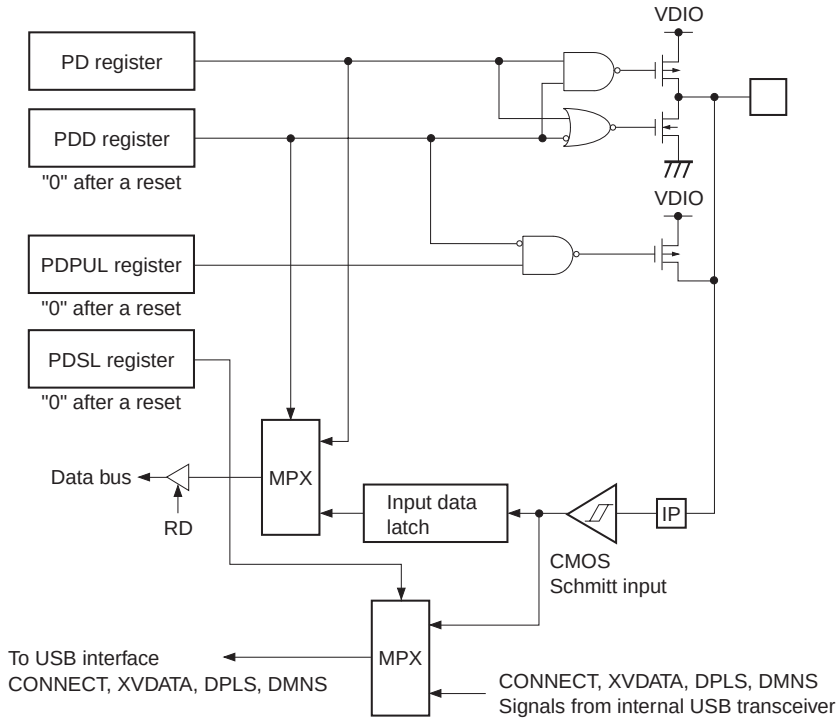
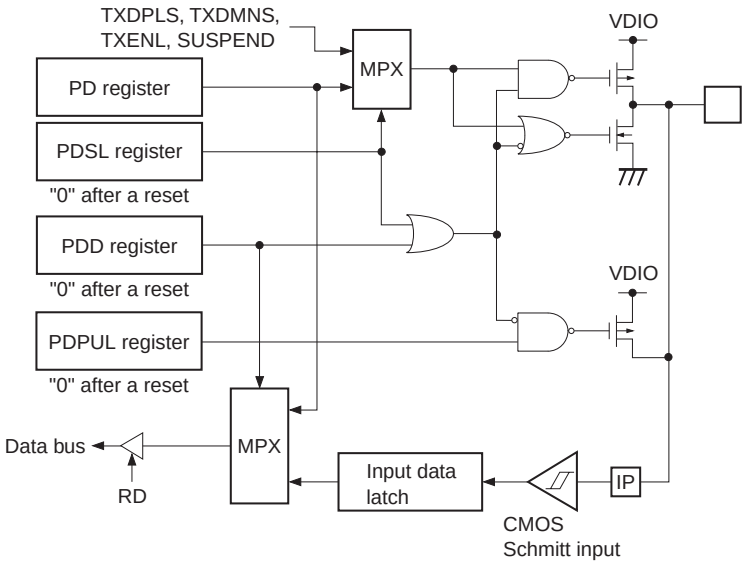
I/O power supply	Digital/Analog	Symbol
VDIO0 VDIO5 VDIO6	Digital power supply	PI0/DADT, PI1/ADDT, PI2/LRCK, PI3/XBCK, PI4/FS256, PI5/MUTFGL, PI6/MUTFGR, PJ0/WAIT, PJ1/RE, PJ2/LWR/LB, PJ3/UWR/UB, PJ4/WE, PK0/CS0, PK1/CS1, PK2, PK3, PK4, PK5/CS5, PK6/CS6, PK7/CS7, PL0/A0 to PL7/A7, PM0/A8 to PM7/A15, PN0/A16 to PN7/A23
VDIODF	Digital power supply	FAD0 to FAD7, FCLE, FALE, FWE, FRE, FWP, FCE0, FRB0, FCE1, FRB1
VDIO1 VDIO2 VDIO3	Digital power supply	PP0, PP1, PO0/D0 to PO7/D7, PB0/D8 to PB7/D15, PA0/PWM, PA1/SDA, PA2/SCL, PC0/SCK0, PC1/SO0, PC2/SI0, PC3/SCS0, KDI, KRB, KCLK, KCS, KDO, TEST4, PE0/TxD0, PE1/RxD0, PE2/TxD1, PE3/RxD1, PE4/SCK1, PE5/SO1, PE6/SI1, PE7/SCS1, TEST5, PF0/EC0/INT3, PF1/T1, PF2/EC2/INT4, PF3/T3, PF4/BEEP, PG0/DACK0, PG1/DREQ0/INT5, PG2/DACK1/INT6, PG3/DREQ1/INT7, TEST0 to TEST3, TEST6, EVA
AVDAD	Analog power supply	AN0 to AN5, AN6/INT8, AN7/INT9 (RST, RAMBK) *1
VDIOJT	Digital power supply	TDI, TMS, TCK, TRST, TDO
VDIO4	Digital power supply	PD0/CONNECT, PD1/XVDATA, PD2/DPLS, PD3/DMNS, PD4/TXDPLS, PD5/TXDMNS, PD6/TXENL, PD7/SUSPEND, VBUS
VDIOUS	Digital power supply	UDM, UDP, TRON
AVDDA	Analog power supply	VREFR, AOUTR, AOUTL, VREFL
AVDMO	Analog power supply	XTAL, EXTAL
AVDUO	Analog power supply	TX, TEX
VDIO7	Digital power supply	PQ0 to PQ7, PR0 to PR7
VDIOMS	Digital power supply	MSDIO, MSBS, MSSCLK, MSINS, PI7

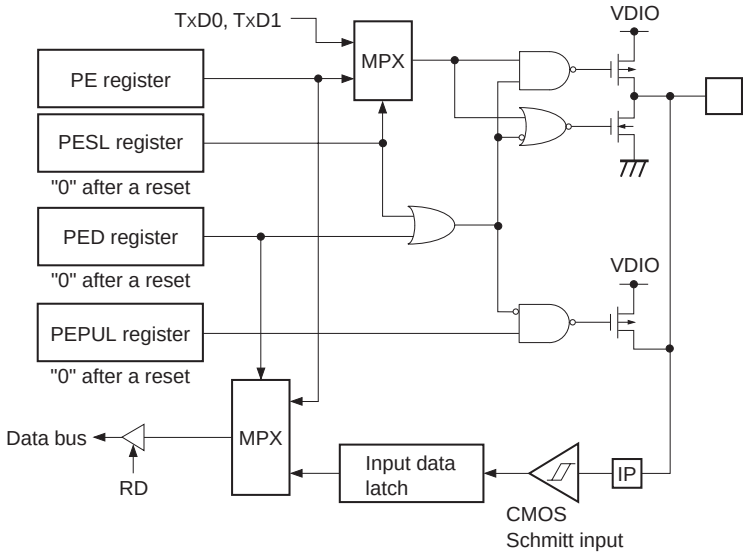
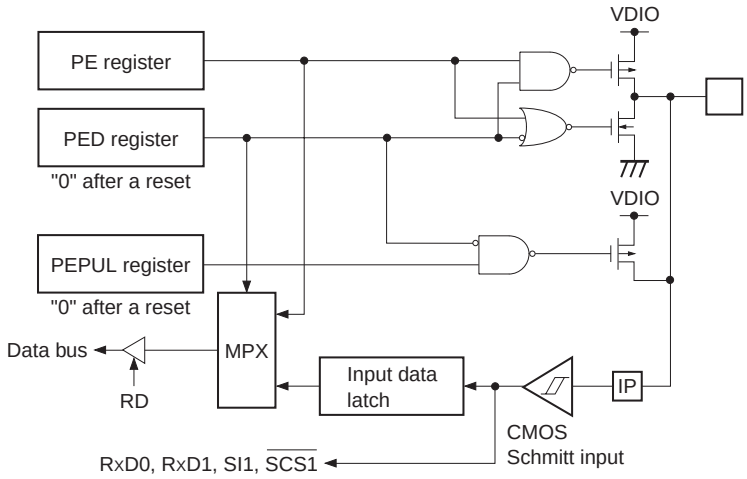
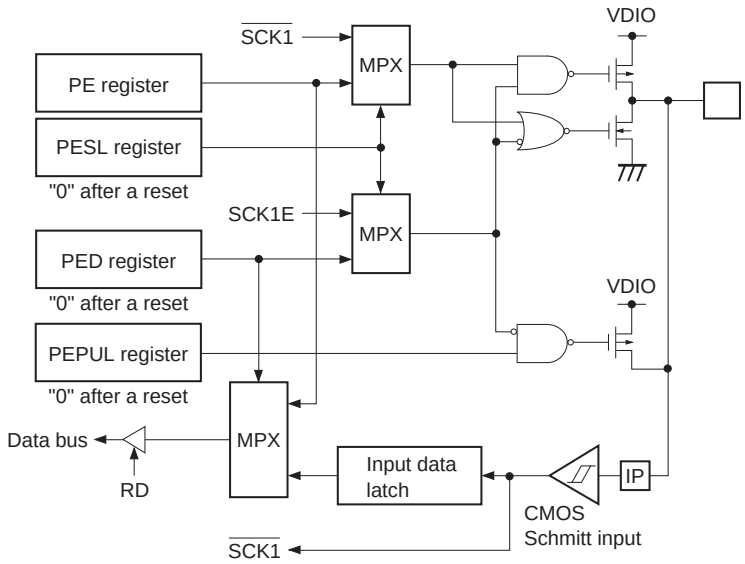
*1 The H level input to RST and RAMBK must be the same potential as $DV_{DD}0$ to $DV_{DD}3$ and VDBK.

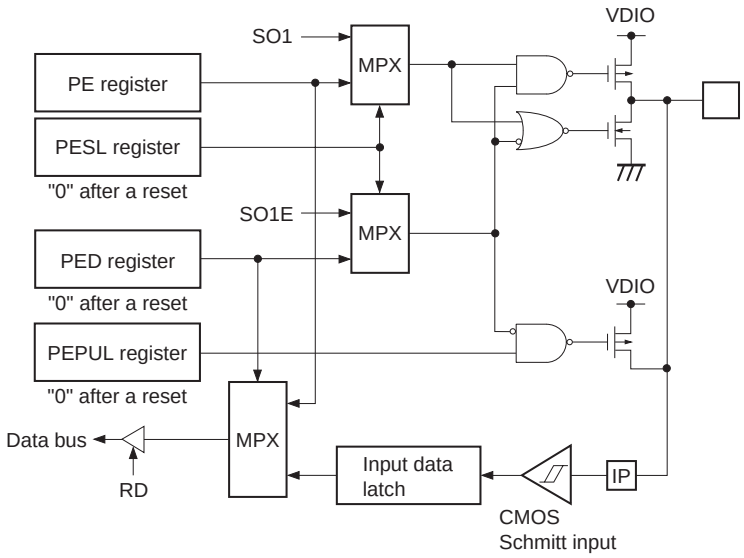
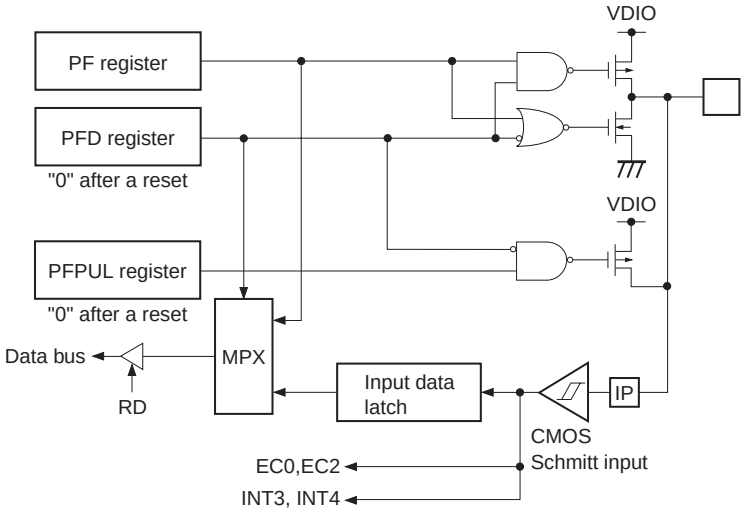
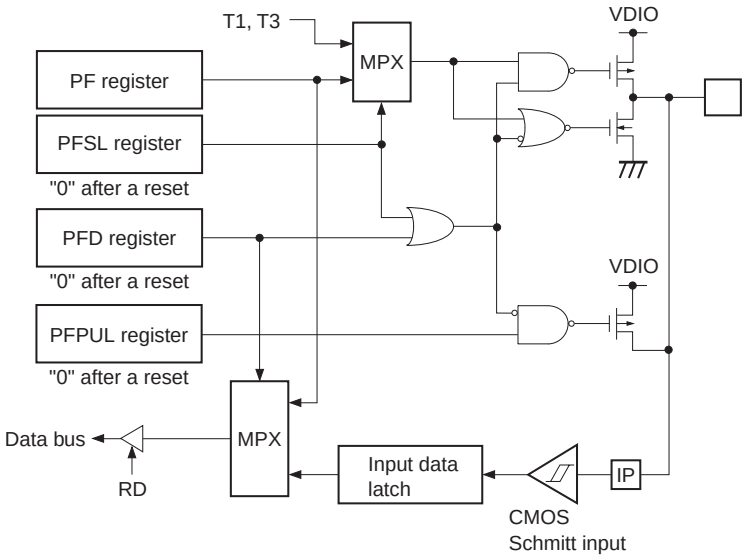
I/O Circuit Format for Pins

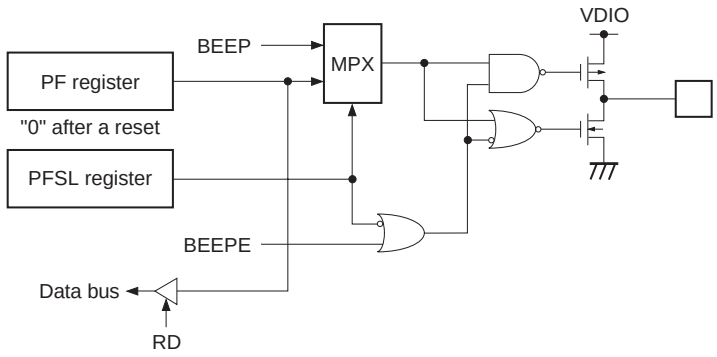
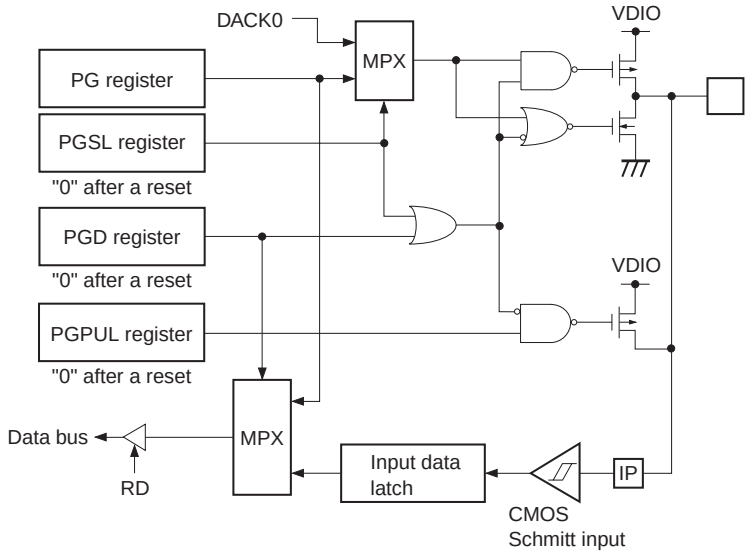
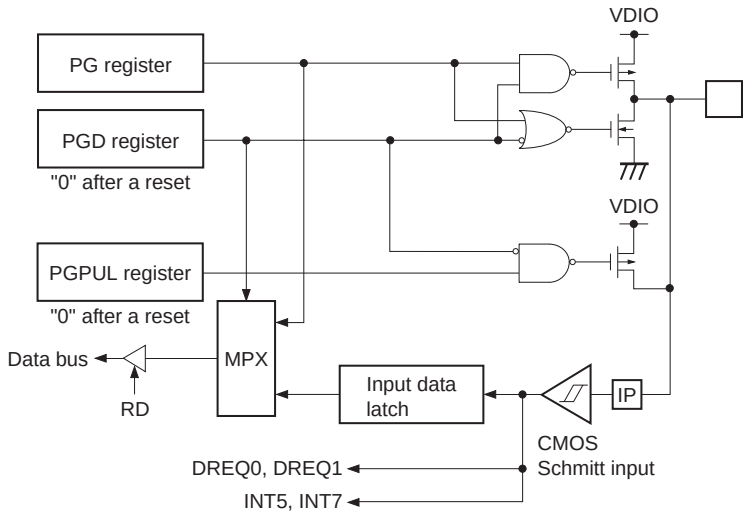
Pin	Circuit format	After a reset
PA0/PWM		Hi-Z
PA1/SDA PA2/SCL		Hi-Z
PB0/D8 to PB7/D15		Hi-Z

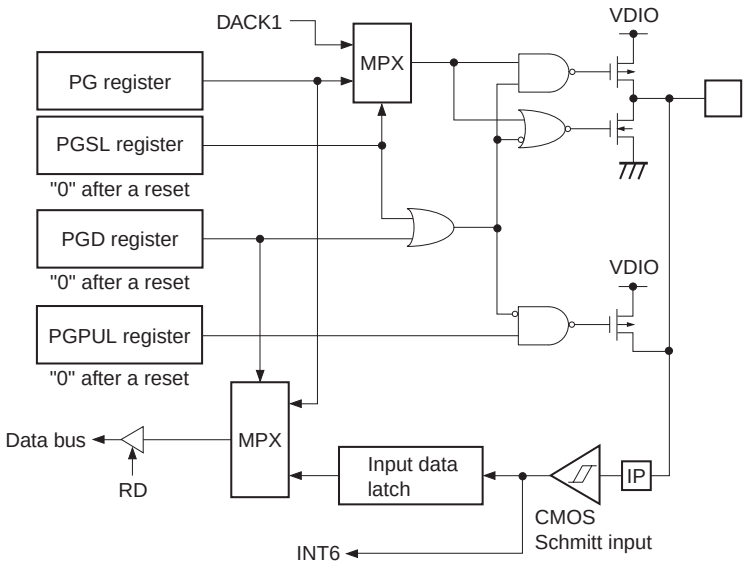
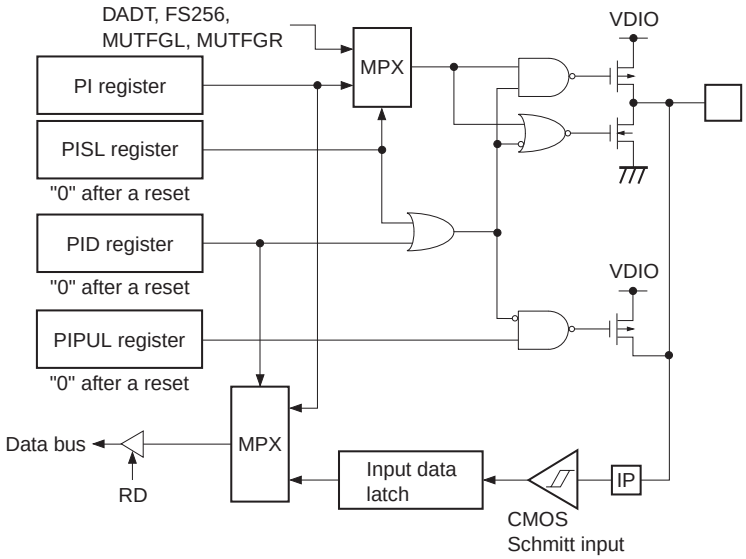
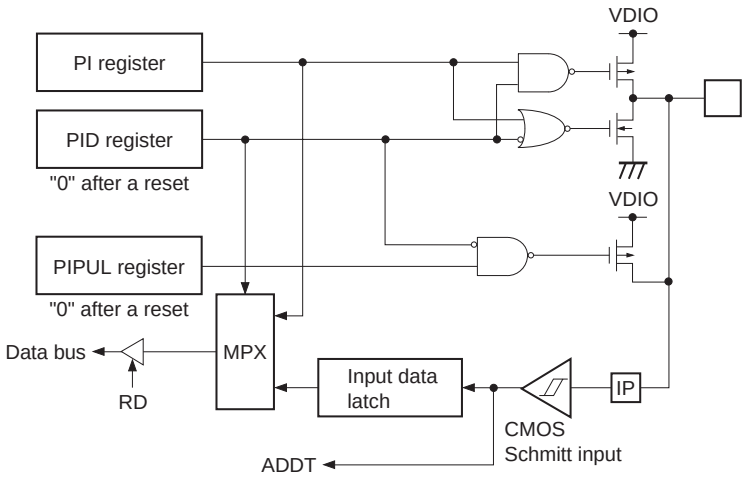
Pin	Circuit format	After a reset
PC0/$\overline{SCK0}$		Hi-Z
PC1/SO0		Hi-Z
PC2/SI0 PC3/$\overline{SCS0}$		Hi-Z

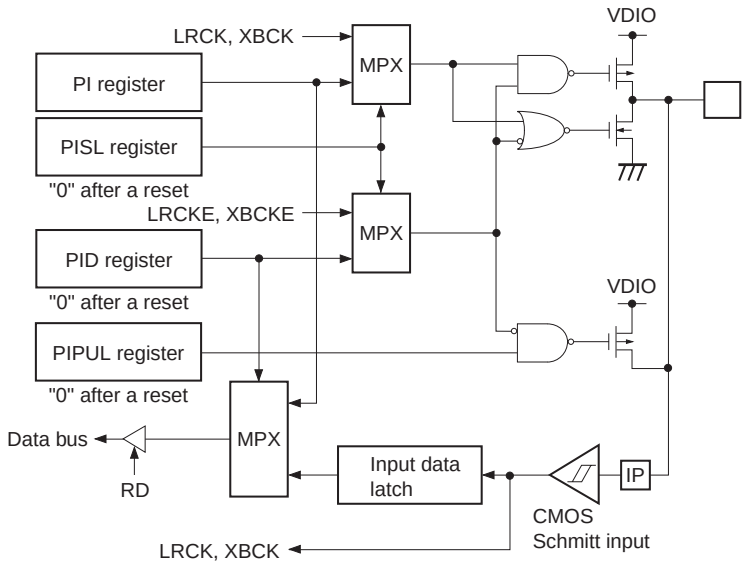
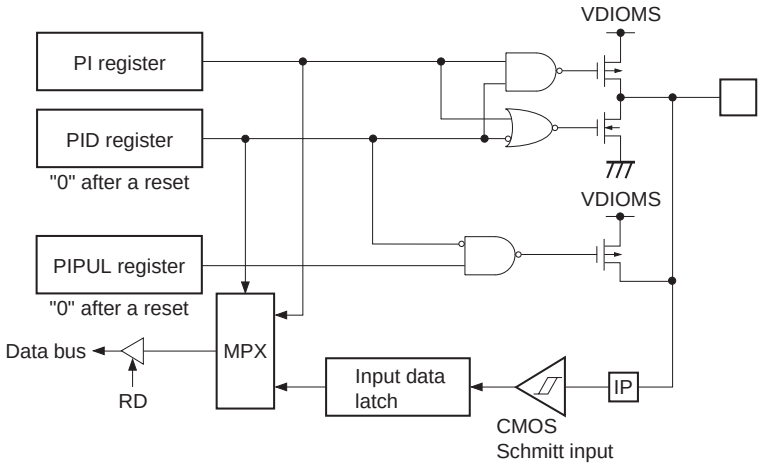
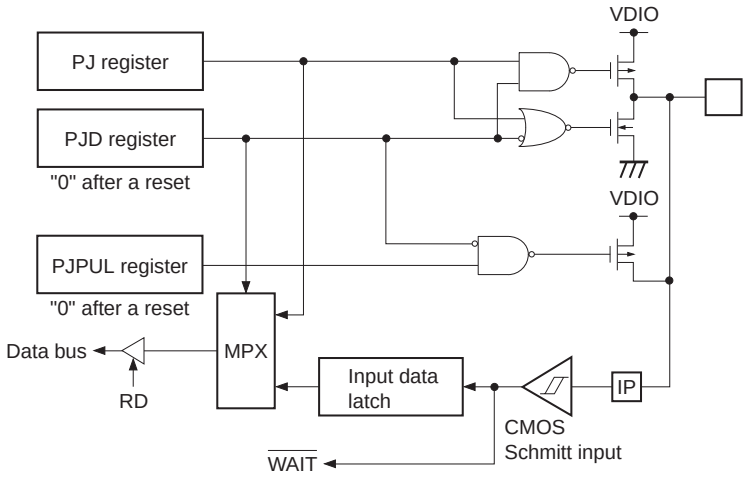
Pin	Circuit format	After a reset
PD0/CONNECT PD1/XVDATA PD2/DPLS PD3/DMNS		Hi-Z
PD4/TXDPLS PD5/TXDMNS PD6/TXENL PD7/SUSPEND		Hi-Z

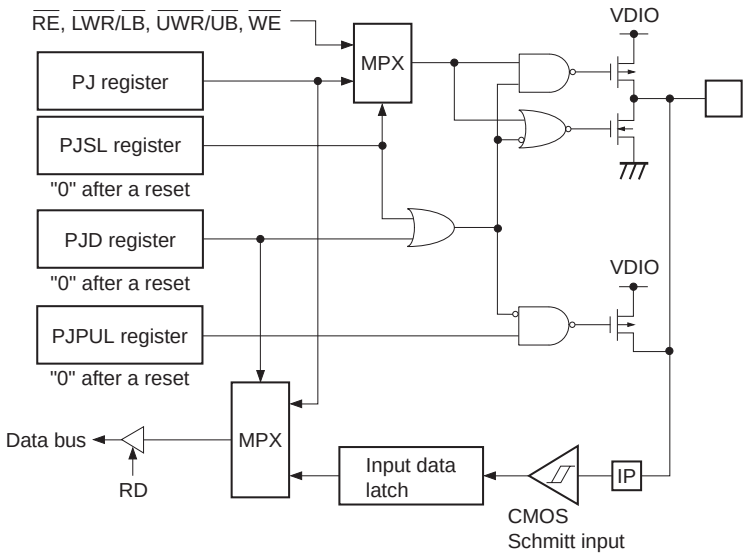
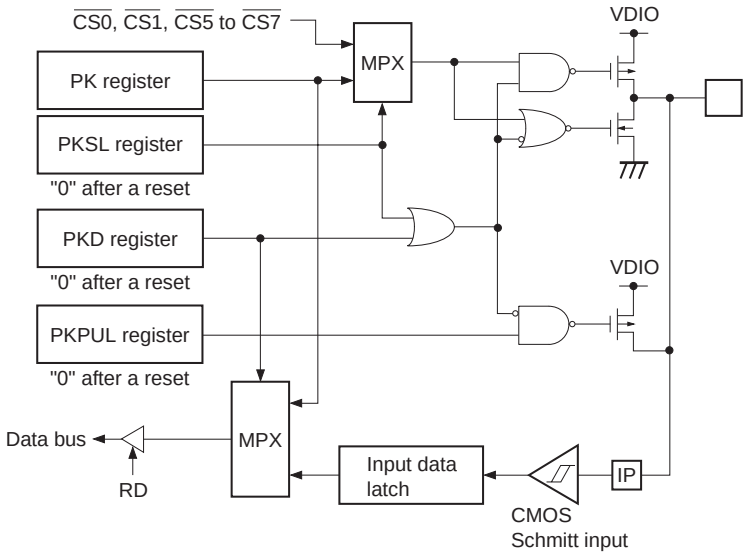
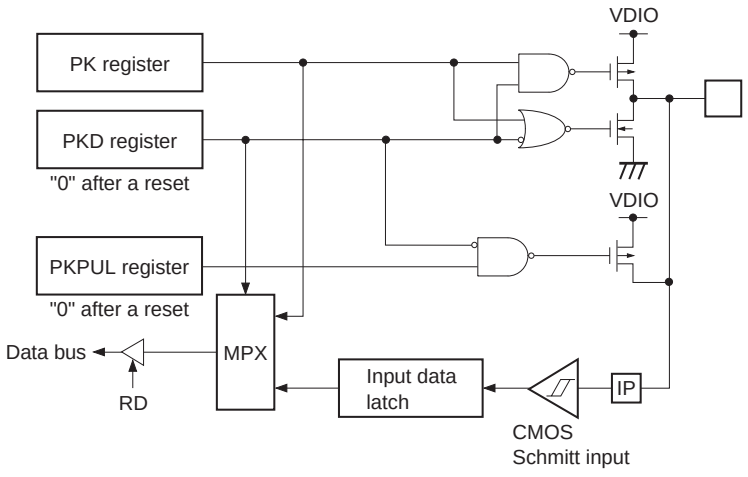
Pin	Circuit format	After a reset
PE0/TxD0 PE2/TxD1		Hi-Z
PE1/RxD0 PE3/RxD1 PE6/SI1 PE7/SCS1		Hi-Z
PE4/SCK1		Hi-Z

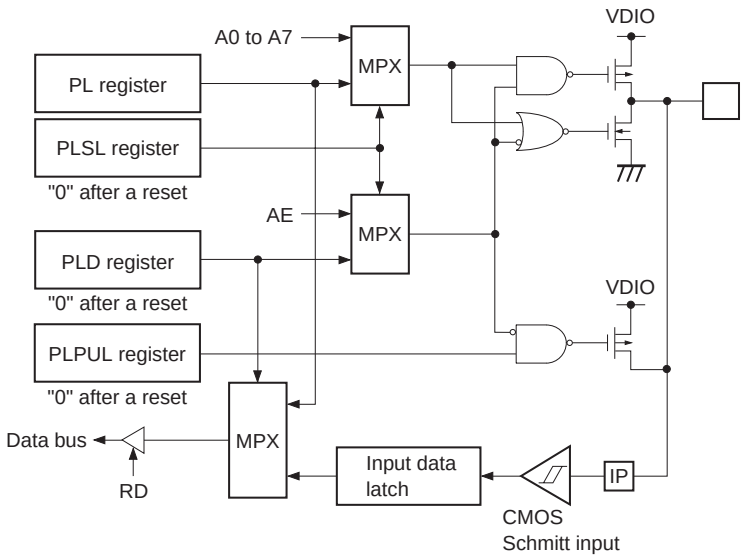
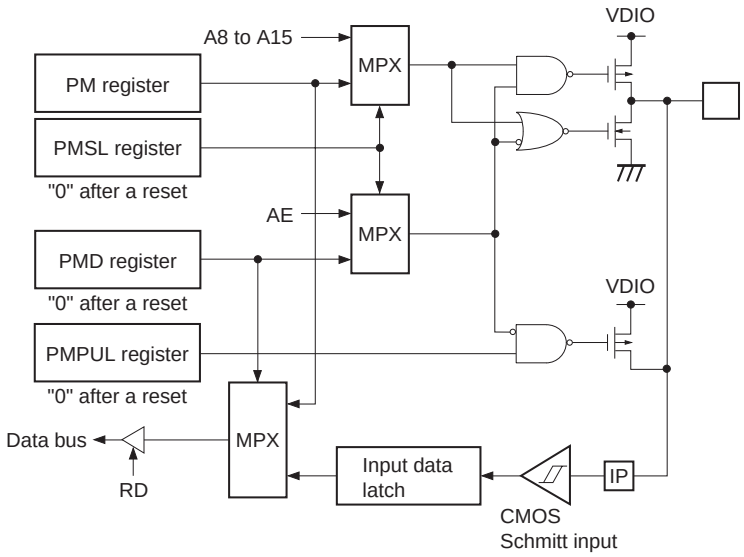
Pin	Circuit format	After a reset
PE5/SO1		Hi-Z
PF0/EC0/INT3 PF2/EC2/INT4		Hi-Z
PF1/T1 PF3/T3		Hi-Z

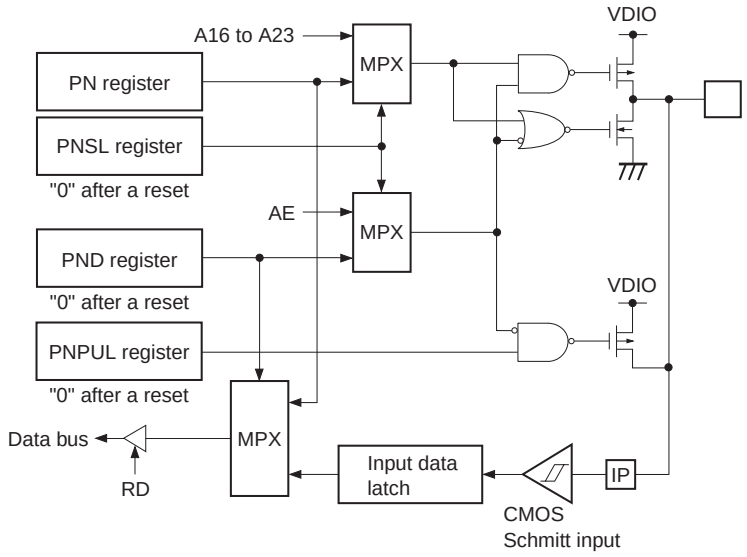
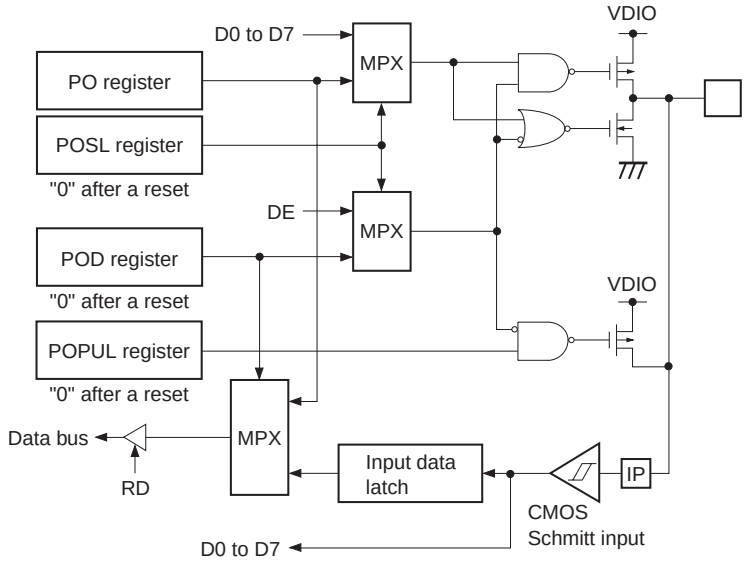
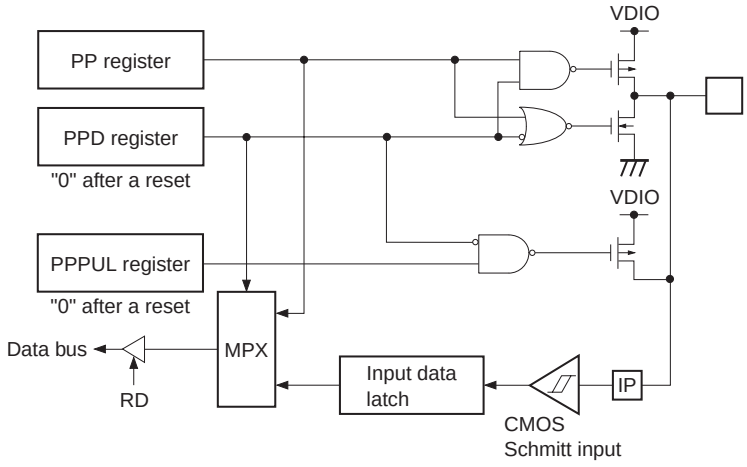
Pin	Circuit format	After a reset
PF4/BEEP		Hi-Z
PG0/DACK0		Hi-Z
PG1/DREQ0/ INT5 PG3/DREQ1/ INT7		Hi-Z

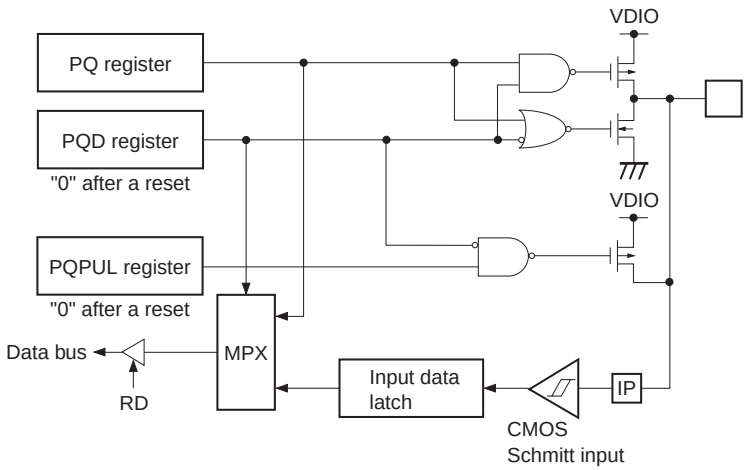
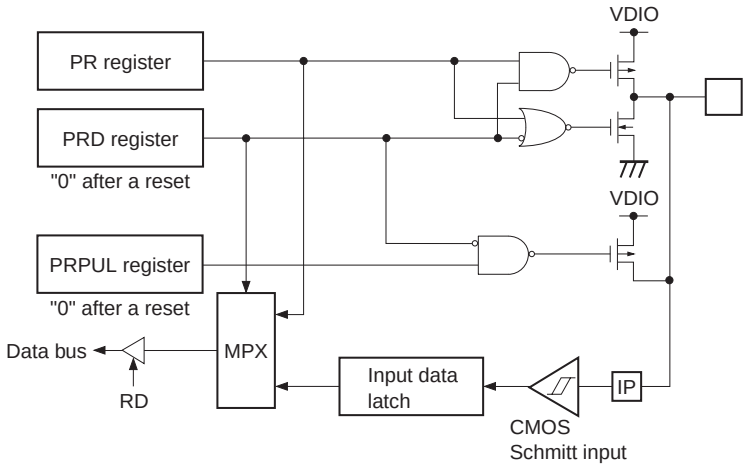
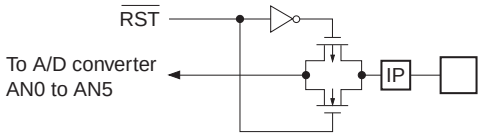
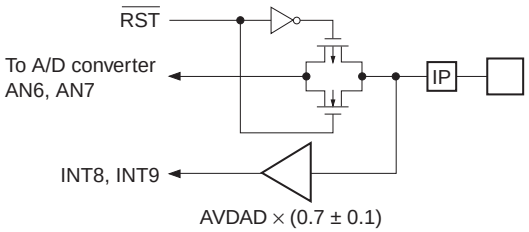
Pin	Circuit format	After a reset
PG2/DACK1/ INT6		Hi-Z
PI0/DADT PI4/FS256 PI5/MUTFGL PI6/MUTFGR		Hi-Z
PI1/ADDT		Hi-Z

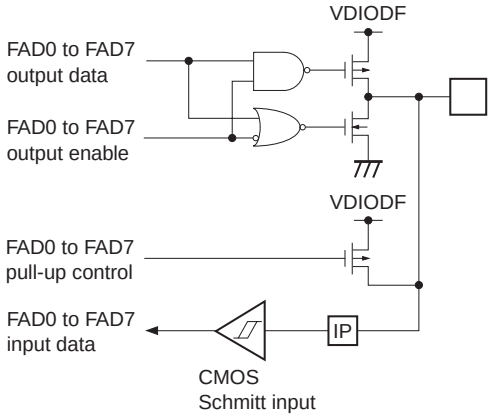
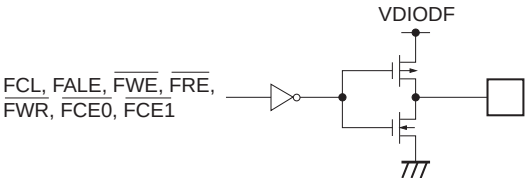
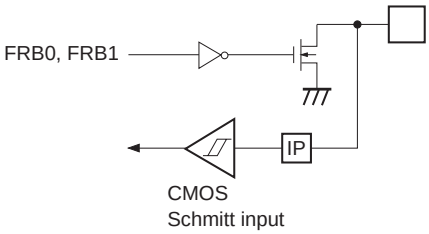
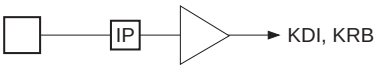
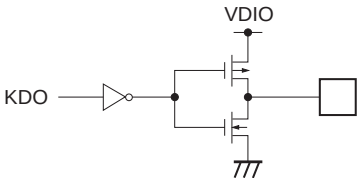
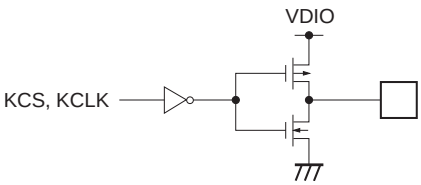
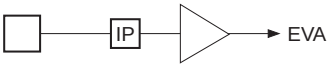
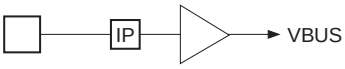
Pin	Circuit format	After a reset
PI2/LRCK PI3/XBCK		Hi-Z
PI7		Hi-Z
PJ0/$\overline{\text{WAIT}}$		Hi-Z

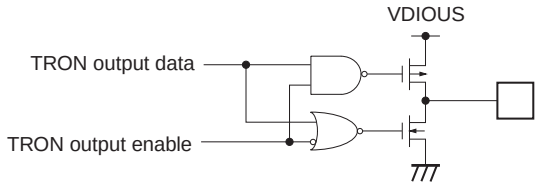
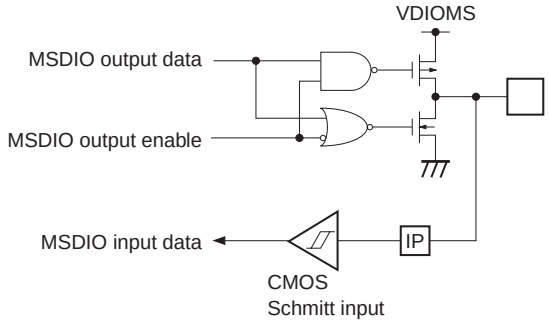
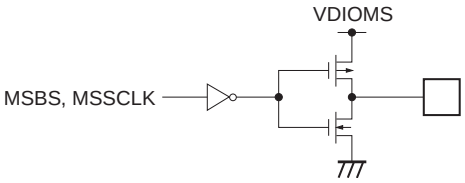
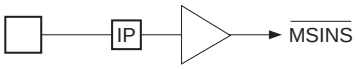
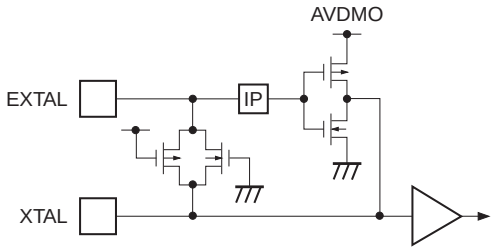
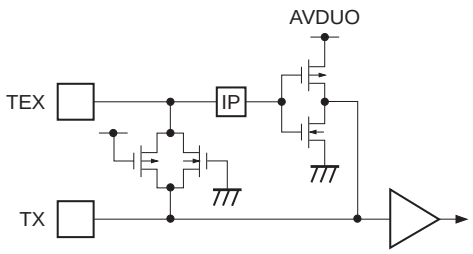
Pin	Circuit format	After a reset
PJ1/$\overline{RE}$ PJ2/$\overline{LWR}$/$\overline{LB}$ PJ3/$\overline{UWR}$/$\overline{UB}$ PJ4/$\overline{WE}$		Hi-Z
PK0/$\overline{CS0}$ to PK1/$\overline{CS1}$ PK5/$\overline{CS5}$ to PK7/$\overline{CS7}$		Hi-Z
PK2 to PK4		Hi-Z

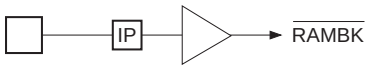
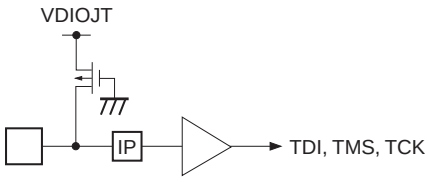
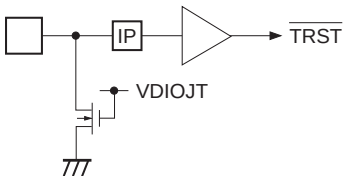
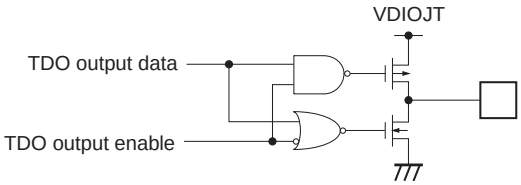
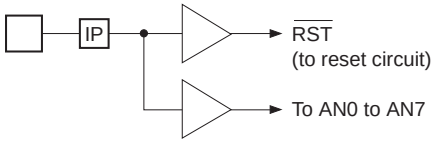
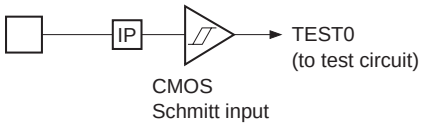
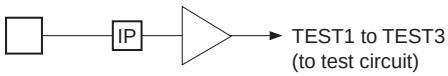
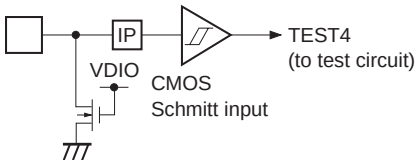
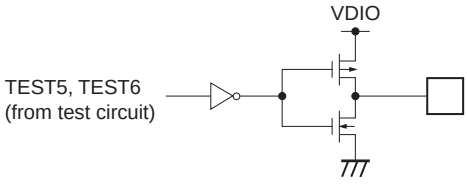
Pin	Circuit format	After a reset
PL0/A0 to PL7/A7		Hi-Z
PM0/A8 to PM7/A15		Hi-Z

Pin	Circuit format	After a reset
PN0/A16 to PN7/A23		Hi-Z
PO0/D0 to PO7/D7		Hi-Z
PP0 PP1		Hi-Z

Pin	Circuit format	After a reset
PQ0 to PQ7		Hi-Z
PR0 to PR7		Hi-Z
AN0 to AN5		Hi-Z
AN6/INT8 AN7/INT9		Hi-Z

Pin	Circuit format	After a reset
FAD0 to FAD7		"L" output
FCLE FALE $\overline{\text{FWE}}$ $\overline{\text{FRE}}$, $\overline{\text{FWR}}$, FCE0, FCE1		"L" output
FRB0 FRB1		"L" output
KDI KRB		Hi-Z
KDO		"L" output
KCS KCLK		"H" output
EVA		Hi-Z
VBUS		Hi-Z

Pin	Circuit format	After a reset
TRON		Hi-Z
MSDIO		Hi-Z
MSBS MSSCLK		"L" output
$\overline{\text{MSINS}}$		Hi-Z
EXTAL XTAL	 • Diagram shows the circuit configuration during oscillation. • XTAL is "H" level when oscillation is stopped.	Oscillation
TEX TX	 • Diagram shows the circuit configuration during oscillation. • TX is "H" level when oscillation is stopped.	Oscillation

Pin	Circuit format	After a reset
$\overline{\text{RAMBK}}$		Hi-Z
TDI TMS TCK		Pull-up
$\overline{\text{TRST}}$		Pull-down
TDO		Hi-Z
$\overline{\text{RST}}$		Hi-Z
TEST0		Hi-Z
TEST1 to TEST3		Hi-Z
TEST4		Pull-down
TEST5 TEST6		"L" output

Absolute Maximum Ratings (DV_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	DV_{DD}	–0.3 to +2.5	V	$DV_{DD}0$, $DV_{DD}1$, $DV_{DD}2$, $DV_{DD}3$
	VDBK	–0.3 to +2.5	V	Power supply for backup RAM
	AVDAD	–0.3 to +4.5	V	
	AVDDA	–0.3 to +4.5	V	
	AVDMO	–0.3 to +4.5	V	
	AVDUO	–0.3 to +4.5	V	
	AVDPLL	–0.3 to +4.5	V	
	VDIO	–0.3 to +4.5	V	VDIO0, VDIO1, VDIO2, VDIO3, VDIO4, VDIO5, VDIO6, VDIO7
	VDIODF	–0.3 to +4.5	V	
	VDIOJT	–0.3 to +4.5	V	
	VDIOUS	–0.3 to +4.5	V	
	VDIOMS	–0.3 to +4.5	V	
Input voltage	V_{IN}	–0.3 to +4.5*1	V	Excludes $\overline{RST}$ and $\overline{RAMBK}$ pins
	V_{INR}	–0.3 to +2.5*2	V	$\overline{RST}$ and $\overline{RAMBK}$ pins
Output voltage	V_{OUT}	–0.3 to +4.5*1	V	
High level output current	I_{OH}	–5	mA	Output (value per pin)
High level total output current	ΣI_{OH}	–40	mA	Total for all output pins
Low level output current	I_{OL}	10	mA	Output (value per pin)
Low level total output current	ΣI_{OL}	80	mA	Total for all output pins
Operating temperature	Topr	–20 to +70	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	380	mW	

*1 V_{IN} and V_{OUT} must not exceed I/O supply voltage (VDIO, VDIODF, VDIOJT, VDIOUS and VDIOMS) + 0.3V.

*2 V_{INR} must not exceed DV_{DD} + 0.3V.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI.
Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (DV_{SS} = 0V reference)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Internal supply voltage	DV_{DD}	1.1		1.3	V	$DV_{DD}0$, $DV_{DD}1$, $DV_{DD}2$, $DV_{DD}3$
Supply voltage for internal RAM backup	VDBK	1.1		1.3	V	*1
AD converter supply voltage	AVDAD	2.2		3.3	V	
DAC supply voltage	AVDDA	2.2		3.3	V	
Main oscillation voltage	AVDMO	2.2		3.3	V	
Sub oscillation voltage	AVDUO	2.7		3.3	V	
PLL voltage	AVDPLL	2.7		3.3	V	
I/O voltage	VDIO	DV_{DD}		3.6	V	VDIO0, VDIO1, VDIO2, VDIO3, VDIO4, VDIO5, VDIO6, VDIO7
JTAG voltage	VDIOJT	1.65		3.3	V	
FLASH I/F voltage with ECC	VDIODF	2.7		3.6	V	
Memory Stick I/F voltage	VDIOMS	2.7		3.6	V	
USB transceiver voltage	VDIOUS	3.0	3.3	3.45	V	
High level input voltage	V_{IHR}	0.7DV_{DD}		DV_{DD}	V	$\overline{RST}$ pin
	V_{IHBK}	0.7VDBK		VDBK	V	$\overline{RAMBK}$ pin
	V_{IHS}	0.7VDIO		VDIO	V	CMOS Schmitt trigger input*2
	V_{IHMSS}	0.7VDIOMS		VDIOMS	V	CMOS Schmitt trigger input*3
	V_{IHDFS}	0.7VDIODF		VDIODF	V	CMOS Schmitt trigger input*4
	V_{IHC}	0.7VDIO		VDIO	V	CMOS input*5
	V_{IHJTC}	0.7VDIOJT		VDIOJT	V	CMOS input*6
	V_{IHMSC}	0.7VDIOMS		VDIOMS	V	CMOS input*7
	V_{IHKW}	0.8AVDAD		AVDAD	V	AN6 and AN7 pins*8
Low level input voltage	V_{ILR}	0		0.2DV_{DD}	V	$\overline{RST}$ pin
	V_{ILBK}	0		0.2VDBK	V	$\overline{RAMBK}$ pin
	V_{ILS}	0		0.2VDIO	V	CMOS Schmitt trigger input*2
	V_{ILMSS}	0		0.2VDIOMS	V	CMOS Schmitt trigger input*3
	V_{ILDFS}	0		0.2VDIODF	V	CMOS Schmitt trigger input*4
	V_{ILC}	0		0.2VDIO	V	CMOS input*5
	V_{ILJTC}	0		0.2VDIOJT	V	CMOS input*6
	V_{ILMSC}	0		0.2VDIOMS	V	CMOS input*7
	V_{ILKW}	0		0.6AVDAD	V	AN6 and AN7 pins*8
Operating temperature	Topr	–20		+70	°C	

*1 VDBK should be the same voltage as DV_{DD} (DV_{DD} ± 0.1V or less).
*2 Each pin of normal input ports (PA to PE, PF0 to PF3, PG, PI0 to PI6, PJ to PR, TEST0).
*3 MSDIO and PI7 pins.
*4 FAD0 to FAD7, FRB0 and FRB1 pins.
*5 KDI, KRB, TEST1 to TEST4, EVA and VBUS pins.
*6 TDI, TMS, TCK and TRST pins.
*7 MSINS pins.
*8 Do not set AN6 and AN7 to the center potential in the steady state.
(Low level input voltage: 0 to 0.4V, High level input voltage: (AVDAD – 0.4V) to AVDAD)

Electrical Characteristics

DC Characteristics

(DV_{DD} = VDBK = 1.1 to 1.3V, AVDAD = AVDDA = AVDMO = 2.2 to 3.3V, AVDUO = AVDPLL = 2.7 to 3.3V)
(VDIO = VDIODF = VDIOMS = 2.7 to 3.6V, VDIOJT = 2.7 to 3.3V, VDIOUS = 3.0 to 3.45V)
(Topr = –20 to +70°C, DV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA0/PWM, PB, PD to PG, PI0 to PI6, PJ to PR *1	VDIO = 2.7V, I_{OH} = –2.0mA	VDIO – 0.4			V
		PI7	VDIOMS = 2.7V, I_{OH} = –2.0mA	VDIOMS – 0.4			V
		D0 to D15, PC0/SCK0, PC1/SO0, PC2, PC3, TXDPLS, TXDMNS, TXENL, SUSPEND, TxD0, TxD1, SCK1, SO1, BEEP, DACK0, DACK1, DADT, LRCK, XBCK, FS256, MUTFGL, MUTFGR, RE, LWR/LB, UWR/UB, WE, CS0, CS1, CS5 to CS7, A0 to A23, KDO, KCLK, KCS *2	VDIO = 2.7V, I_{OH} = –4.0mA	VDIO – 0.4			V
		TDO	VDIOJT = 2.7V, I_{OH} = –4.0mA	VDIOJT – 0.4			V
		TRON	VDIOUS = 3.0V, I_{OH} = –4.0mA	VDIOUS – 0.4			V
		MSDIO, MSBS, MSSCLK	VDIOMS = 2.7V, I_{OH} = –4.0mA	VDIOMS – 0.4			V
		FAD0 to FAD7, FCLE, FALE, FWE, FRE, FWP, FCE0, FCE1	VDIODF = 2.7V, I_{OH} = –4.0mA	VDIODF – 0.4			V
Low level output voltage	V_{OL}	PA0/ PWM, PB, PD to PG, PI0 to PI6, PJ to PR *1	VDIO = 2.7V, I_{OL} = 2.0mA			0.4	V
		PI7	VDIOMS = 2.7V, I_{OL} = 2.0mA			0.4	V
		FRB0, FRB1	VDIODF = 2.7V, I_{OL} = 2.0mA			0.4	V
		PA1/ SDA, PA2/SCL, D0 to D15, PC0/SCK0, PC1/SO0, PC2, PC3, TXDPLS, TXDMNS, TXENL, SUSPEND, TxD0, TxD1, SCK1, SO1, BEEP, DACK0, DACK1, DADT, LRCK, XBCK, FS256, MUTFGL, MUTFGR, RE, LWR/LB, UWR/UB, WE, CS0, CS1, CS5 to CS7, A0 to A23, KDO, KCLK, KCS *2	VDIO = 2.7V, I_{OL} = 4.0mA			0.4	V
		TDO	VDIOJT = 2.7V, I_{OL} = 4.0mA			0.4	V

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Low level output voltage	V_{OL}	TRON	VDIOUS = 3.0V, I_{OL} = 4.0mA			0.4	V
		MSDIO, MSBS, MSSCLK	VDIOMS = 2.7V, I_{OL} = 4.0mA			0.4	V
		FAD0 to FAD7, FCLE, FALE, $\overline{FWE}$, $\overline{FRE}$, $\overline{FWP}$, $\overline{FCE0}$, $\overline{FCE1}$	VDIODF = 2.7V, I_{OL} = 4.0mA			0.4	V
Input current	I_{IL}*3	PA to PG, PI0 to PI6, PJ to PR	VDIO = 2.7V, V_{IL} = V_{SS}	–30			µA
			VDIO = 3.6V, V_{IL} = V_{SS}			–150	µA
		PI7	VDIOMS = 2.7V, V_{IL} = V_{SS}	–30			µA
			VDIOMS = 3.6V, V_{IL} = V_{SS}			–150	µA
		FAD0 to FAD7	VDIODF = 2.7V, V_{IL} = V_{SS}	–30			µA
			VDIODF = 3.6V, V_{IL} = V_{SS}			–150	µA
I/O leakage current	I_{ZH}*3	PA to PG, PI0 to PI6, PJ to PR, KDI, KRB, KDO, KCLK, KCS, TEST0 to TEST6, EVA, VBUS	VDIO = 3.6V, V_I = 3.6V			10	µA
		TDO	VDIOJT = 3.3V, V_I = 3.3V			10	µA
		TRON	VDIOUS = 3.45V, V_I = 3.45V			10	µA
		PI7, MSDIO, MSBS, MSSCLK, $\overline{MSINS}$	VDIOMS = 3.6V, V_I = 3.6V			10	µA
		FAD0 to FAD7, FCLE, FALE, $\overline{FWE}$, $\overline{FRE}$, $\overline{FWP}$, $\overline{FCE0}$, $\overline{FCE1}$, FRB0, FRB1	VDIODF = 3.6V, V_I = 3.6V			10	µA
		AN0 to AN7	AVDAD = 3.3V, V_I = 3.3V			10	µA
		$\overline{RAMBK}$, $\overline{RST}$	VDBK = 1.3V, V_I = 1.3V			10	µA
	I_{ZL}	PA to PG, PI0 to PI6, PJ to PR, KDI, KRB, KDO, KCLK, KCS, TEST0 to TEST6, EVA, VBUS	VDIO = 3.6V, V_I = 0V			–10	µA
		TDO	VDIOJT = 3.3V, V_I = 0V			–10	µA
		TRON	VDIOUS = 3.45V, V_I = 0V			–10	µA
		PI7, MSDIO, MSBS, MSSCLK, $\overline{MSINS}$	VDIOMS = 3.6V, V_I = 0V			–10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
I/O leakage current	I_{ZL}	FAD0 to FAD7, FCLE, FALE, FWE, FRE, FWP, FCE0, FCE1, FRB0, FRB1	VDIODF = 3.6V, V_I = 0V			–10	µA
		AN0 to AN7	AVDAD = 3.3V, V_I = 0V			–10	µA
		RAMBK, RST	VDBK = 1.3V, V_I = 0V			–10	µA
Input capacitance	C_{IN}	PA to PG, PI to PR, AN0 to AN7, FAD0 to FAD7, FRB0, FRB1, MSDIO, MSINS, KRB, KDI, EVA, TEST0 to TEST4, RAMBK, RST	Clock 1MHz 0V except the measured pins			11	pF

*1 When used as PA0/PWM, PB, PD to PG and PI to PO, specified at I_{OH} = –2.0mA and I_{OL} = 2.0mA.

*2 When used as PA1/SDA, PA2/SCL, PC and dual function pins, specified at I_{OH} = –4.0mA and I_{OL} = 4.0mA.

*3 The PA to PG, PI to PR and FAD0 to FAD7 pins specify the input current when the pull-up resistor is selected, and specify the leakage current when non-resistor is selected.

(Topr = –20 to +70°C, DV_{DD} = 1.1 to 1.3V, DVss = 0V reference)

Item	Pins	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply current*1	DV_{DD}/VDBK	$I_{DD}1$	Main execution mode*2 f_{SRC} = 22.58MHz crystal oscillation 1/2 frequency division (11.29MHz) (C_1 = C_2 = 10pF)*4		—	4.5	7.5	mA
		$I_{DD}2$	Main execution mode*3 f_{SRC} = 22.58MHz crystal oscillation (C_1 = C_2 = 10pF)*4		—	—	29	mA
		$I_{DD}I$	Main idle mode f_{SRC} = 22.58MHz crystal oscillation (C_1 = C_2 = 10pF)*4		—	3.5	6.5	mA
		$I_{DD}S1$	Stop mode	Ta = 25°C (DV_{DD} = 1.2V)	—	100	300	µA
		$I_{DD}S2$		Ta = –20 to +50°C		—	1500	

*1 When all output pins are left open, this indicates the current flowing to DV_{DD} and VDBK.

*2 During ATRAC3 decoding operation.

*3 When the arithmetic accelerator circuit is always operating.

*4 C_1 and C_2 indicate the external capacitors attached to the EXTAL and XTAL pins, respectively.

AC Characteristics

(1) EXTAL pins

1) Automatic oscillation

(Topr = –20 to +70°C, DV_{DD} = VDBK = 1.1 to 1.3V, AVDMO = 2.2 to 3.3V, AVSOSC = DVss = 0V reference)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{SRC}		22.4	22.5792	22.8	MHz

2) When inputting pulses to EXTAL pin

(Topr = –20 to +70°C, DV_{DD} = VDBK = 1.1 to 1.3V, AVDMO = 2.2 to 3.3V, AVSOSC = DVss = 0V reference)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}		16			ns
Low level pulse width	t_{WLX}		16			ns
Pulse period	t_{CX}		43.9		44.6	ns
Input high level	V_{IHX}		0.7AVDMO			V
Input low level	V_{ILX}				0.2AVDMO	V
Rise time, fall time	t_R, t_F				7	ns

Note) When the clock is supplied externally, input to the EXTAL pin and input an opposite phase clock to the XTAL pin.

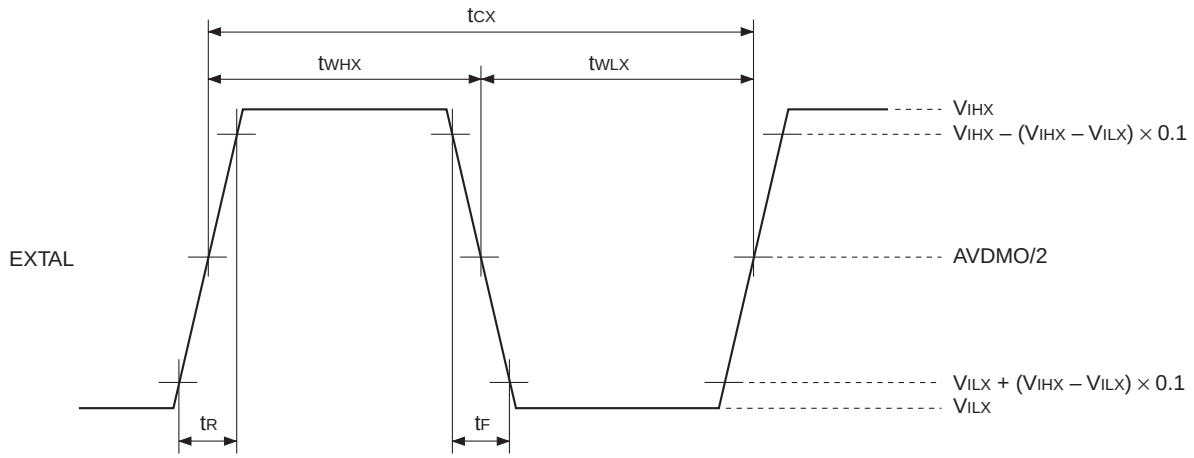


Fig. 1. Main Clock Timing

(2) TEX pin

1) Automatic oscillation

(Topr = –20 to +70°C, DV_{DD} = VDBK = 1.1 to 1.3V, AVDUO = 2.7 to 3.3V, AVSOSC = DVss = 0V reference)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{TEX}		8		16	MHz

2) When inputting pulses to TEX pin

(Topr = –20 to +70°C, DV_{DD} = VDBK = 1.1 to 1.3V, AVDUO = 2.7 to 3.3V, AVSOSC = DVss = 0V reference)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHTX}		25			ns
Low level pulse width	t_{WLTX}		25			ns
Pulse period	t_{CTX}		62.5		125	ns
Input high level	V_{IHTX}		0.7AVDUO			V
Input low level	V_{ILTX}				0.2AVDUO	V
Rise time, fall time	t_R, t_F				7	ns

Note) When the clock is supplied externally, input to the TEX pin and input an opposite phase clock to the TX pin.

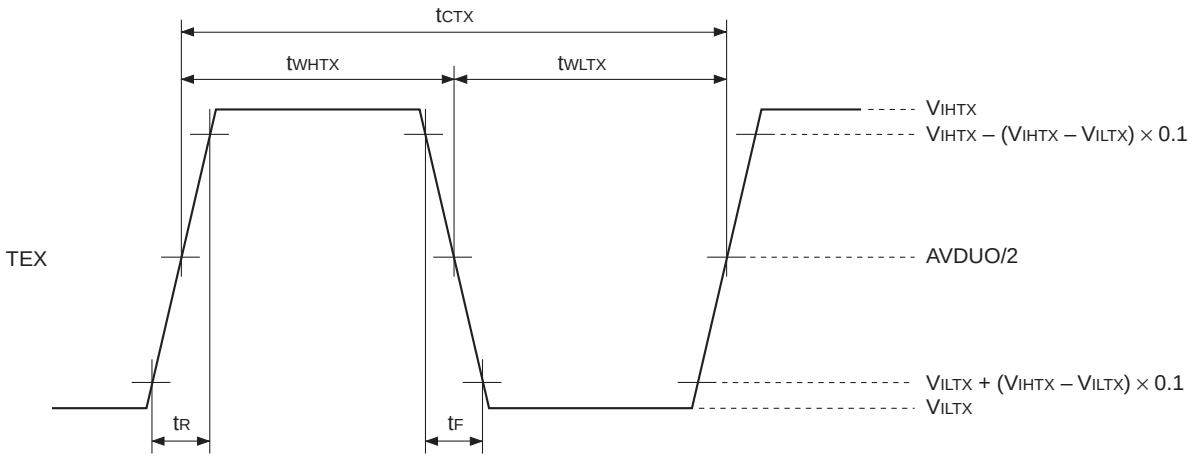


Fig. 2. Sub Clock Timing

3) Serial transfer (CH0, CH1)

(Topr = –20 to +70°C, DV_{DD} = 1.1 to 1.3V, VDIO = 2.7 to 3.3V, DV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	$6/f_{PS2}$	—	ns
		$\overline{SCK1}$	Output mode	$1/f_{SCK}$	—	ns
$\overline{SCK}$ high, low pulse width	t_{KH}	$\overline{SCK0}$	Input mode	$3/f_{PS2}$	—	ns
	t_{KL}	$\overline{SCK1}$	Output mode	$0.5/f_{SCK} – 5$	—	ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI0	$\overline{SCLK}$ input mode	$–2/f_{PS2} + 5$	—	ns
		SI1	$\overline{SCLK}$ output mode	35	—	ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI0	$\overline{SCLK}$ input mode	$2/f_{PS2} + 5$	—	ns
		SI1	$\overline{SCLK}$ output mode	0	—	ns
$\overline{SCK}\downarrow \rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCLK}$ input mode	—	$3/f_{PS2} + 40$	ns
		SO1	$\overline{SCLK}$ output mode	—	5	ns

Note 1) The load capacitance of the measurement pin is 75pF.

Note 2) f_{SCK}: Serial clock

Note 3) f_{PS2}: PS2 clock ($f_{PS2} = f_{SRC}/4$)

Note 4) $f_{SCK} = f_{PS2}/\{2 \times (\text{Register setting value} + 1)\}$: Register setting value (01h to FFh)

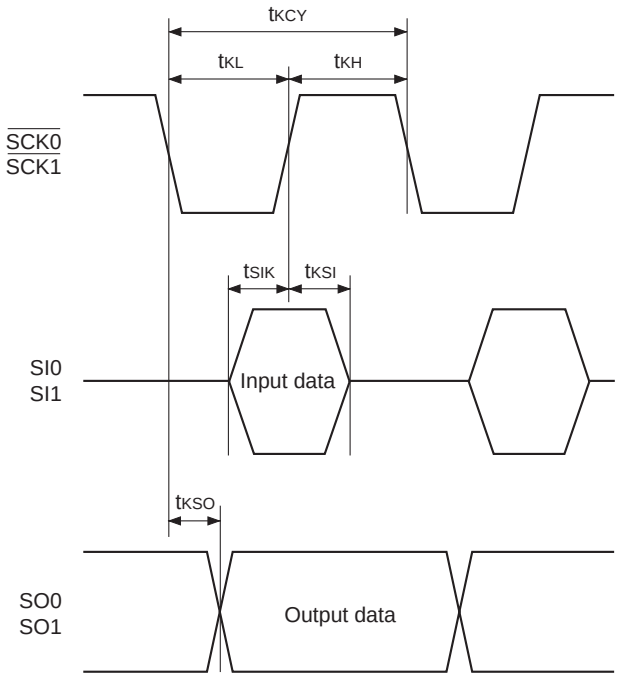


Fig. 3. Serial CH0 and CH1 Transfer Timing

4) Serial transfer (Memory Stick)

(Topr = –20 to +70°C, DV_{DD} = 1.1 to 1.3V, VDIOMS = 2.7 to 3.6V, DV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
MSSCLK cycle time	t_{KCY}	MSSCLK		$1000/f_{MSCK}$	—	ns
MSSCLK high, low pulse width	t_{KH}, t_{KL}	MSSCLK		$500/f_{MSCK}$ – 5	—	ns
MSBS output delay time	t_{BSD}	MSBS	For MSSCLK↓	—	10	ns
MSDIO output delay time	t_{DIOD}	MSDIO	For MSSCLK↓	—	10	ns
MSDIO input setup time	t_{DIOS}	MSDIO	For MSSCLK↑	14	—	ns
MSDIO input hold time	t_{DIOH}	MSDIO	For MSSCLK↑	5	—	ns

Note 1) The load capacitance is 26pF.

Note 2) The oscillation of the TEX pin is at 50% duty.

Note 3) f_{MSCK} is as follows for f_{SRC} from the main oscillation circuit or f_{TEX} from the sub oscillation circuit.

Shift clock frequency division ratio	f_{MSCK} [MHz]
Main oscillation 1/2 frequency division	$f_{SRC}/2$
Main oscillation 1/4 frequency division	$f_{SRC}/4$
Sub oscillation	f_{TEX}

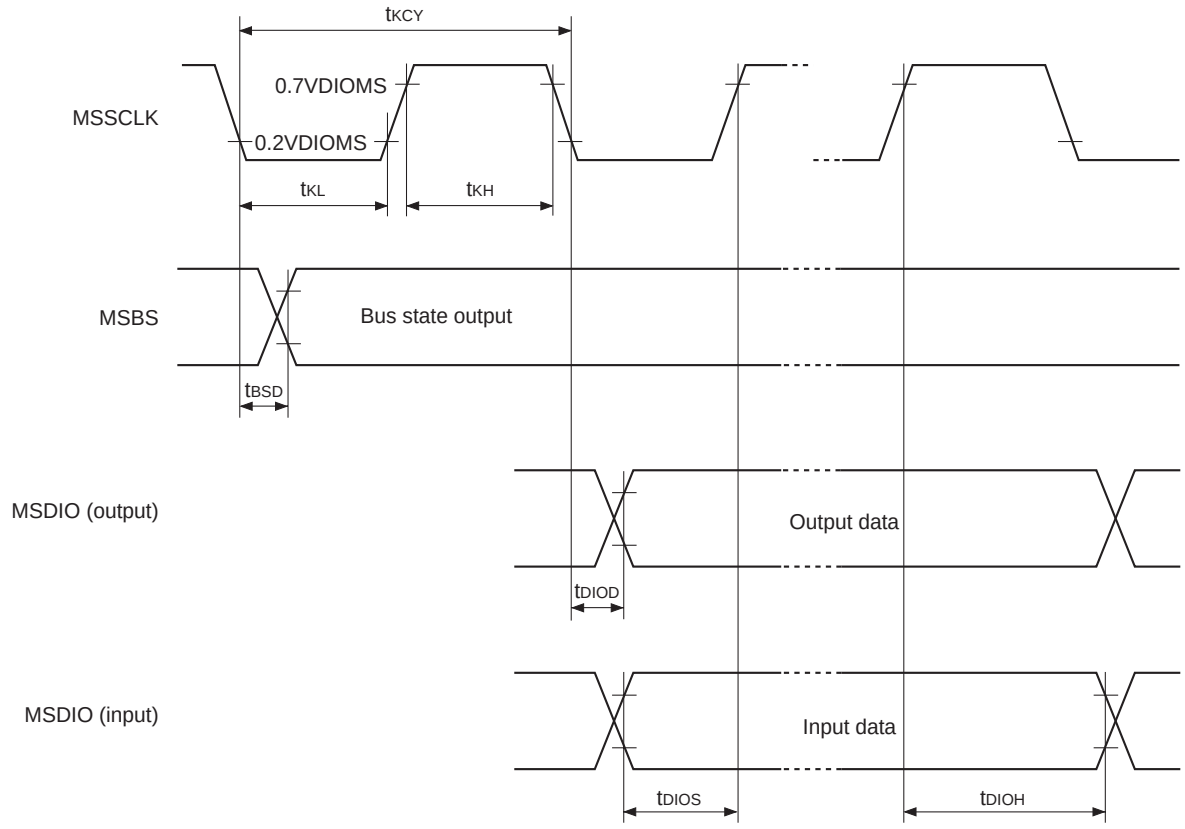


Fig. 4. Memory Stick Transfer Timing

5) Flash memory interface characteristics

(Topr = –20 to +70°C, DV_{DD} = 1.1 to 1.3V, VDIODF = 2.7 to 3.3V, DV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{FRE}$ low pulse width	t_{RECY}	$\overline{FRE}$		T × (RSTB setting value) – 10	—	ns
$\overline{FRE}\uparrow$ setup time	t_{RSFA}	FAD[7:0]		35	—	ns
$\overline{FRE}\uparrow$ hold time	t_{RHFA}	FAD[7:0]		0	—	ns
$\overline{FEW}$ low pulse width	t_{WECY}	$\overline{FWE}$		T × (WSTB setting value) – 10	—	ns
$\overline{FWE}\uparrow$ setup time	t_{WSFA}	FAD[7:0]		T × (WSTP setting value + WSTB setting value) – 10	—	ns
$\overline{FWE}\uparrow$ hold time	t_{WHFA}	FAD[7:0]		T × (WHLD setting value) – 10	—	ns

Note 1) "T" indicates the 1 cycle (1/f_{SRC}) of the system clock.

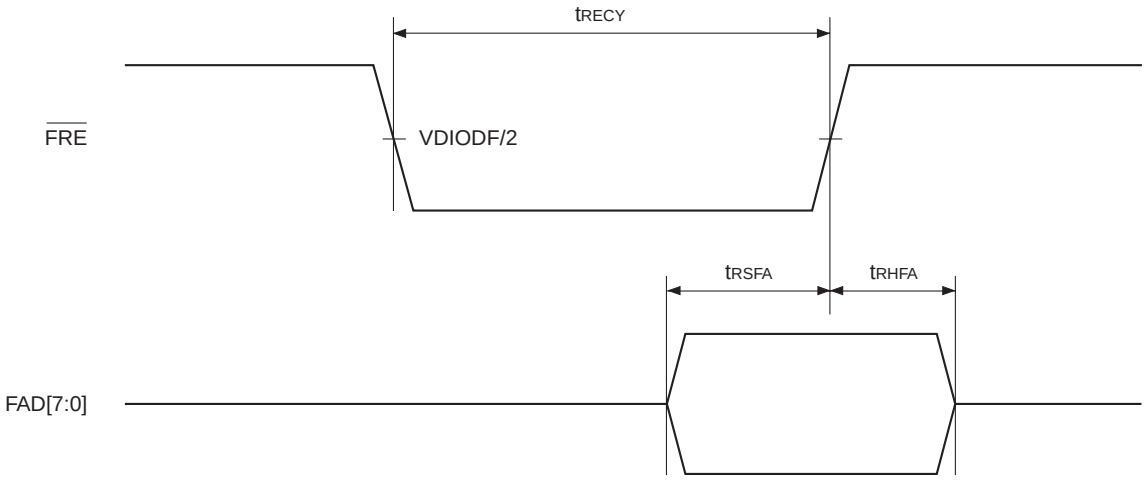
Note 2) RSTB, WSTB, WSTP and WHLD indicate the register set to the flash memory interface WE/RE timing register (FIWERETR).
See the table below for allowable setting values.

Note 3) The load capacitance of the measurement pin is 75pF.

RSTB, WSTB, WSTP and WHLD setting value

Item	Bits within FIWERETR register	Allowable setting values
WSTP	[27:24]	0h to Fh
WSTB	[23:20]	0h to Fh
WHLD	[19:16]	0h to Fh
RSTB	[7:4]	0h to Fh

• **During Read**



• **During Write**

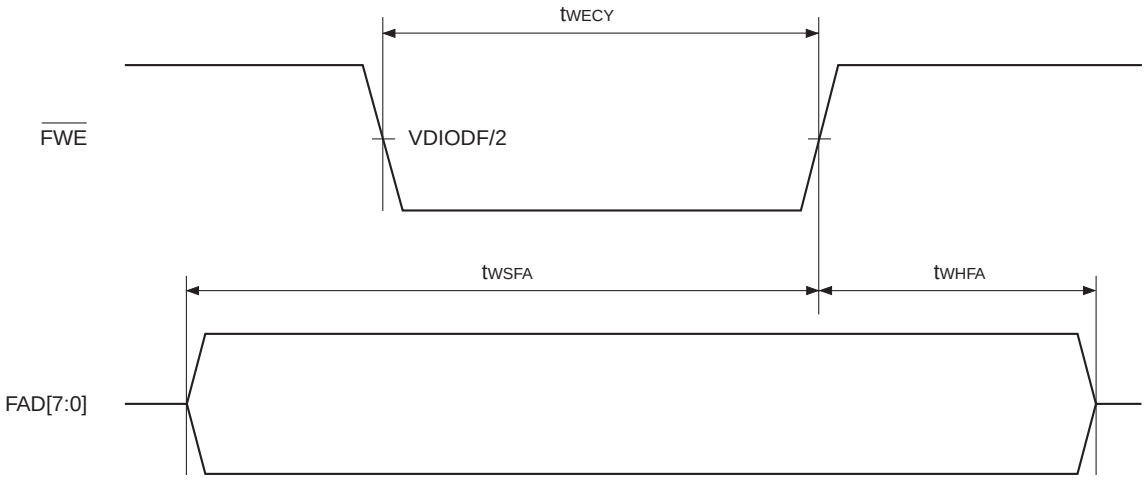


Fig. 5. Flash Memory Interface Transfer Timing with ECC

6) Bus interface unit (BIU) characteristics

• 2-cycle access AC characteristics parameter in write operation

(Topr = –20 to +70°C, DV_{DD} = 1.1 to 1.3V, VDIO = 2.7 to 3.3V, DV_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit
Address setup time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↓	t_{ADULD1}	$3/2f_{SRC}$ – 5	—	ns
$\overline{CS}$↓ and $\overline{WE}$↓ setup time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↓	t_{CWULD1}	$3/2f_{SRC}$ – 5	—	ns
Address hold time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↑	t_{ULADD1}	$1/2f_{SRC}$ – 5	—	ns
$\overline{CS}$↑ and $\overline{WE}$↑ hold time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↑	t_{ULCWD1}	$1/2f_{SRC}$ – 5	—	ns
$\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) low pulse width	t_{WUL1}	$1/f_{SRC}$	—	ns
Data setup time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↓	t_{DULD1}	$1/2f_{SRC}$ – 5	—	ns
Data hold time for $\overline{CS}$↑ and $\overline{WE}$↑	t_{DD1}	0	—	ns

Note) The load capacitance of the measurement pin is 75pF.

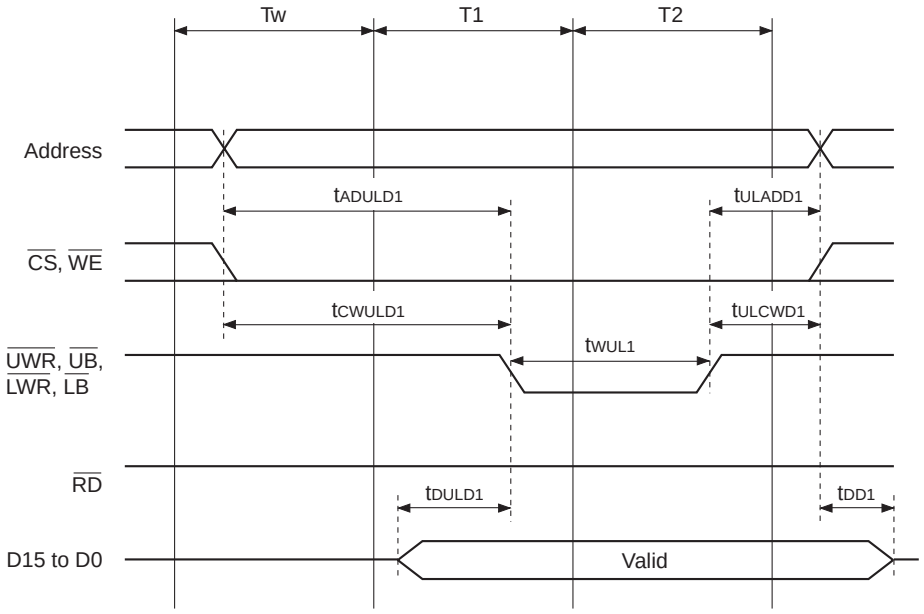


Fig. 6. 2-cycle Access Basic Timing in Write Operation

• 3-cycle access AC characteristics parameter in write operation

(Topr = –20 to +70°C, DV_{DD} = 1.1 to 1.3V, VDIO = 2.7 to 3.3V, DV_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit
Address setup time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↓	t_{ADULD2}	$2/f_{SRC}$ – 5	—	ns
$\overline{CS}$↓ and $\overline{WE}$↓ setup time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↓	t_{CWULD2}	$2/f_{SRC}$ – 5	—	ns
Address hold time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↑	t_{ULADD2}	$1/f_{SRC}$ – 5	—	ns
$\overline{CS}$↑ and $\overline{WE}$↑ hold delay time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↑	t_{ULCWD2}	$1/f_{SRC}$ – 5	—	ns
$\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) low pulse width	t_{WUL2}	$1/f_{SRC}$	—	ns
Data setup time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↓	t_{DULD2}	$1/f_{SRC}$ – 5	—	ns
Data hold time for $\overline{CS}$↑ and $\overline{WE}$↑	t_{DD2}	0	—	ns

Note) The load capacitance of the measurement pin is 75pF.

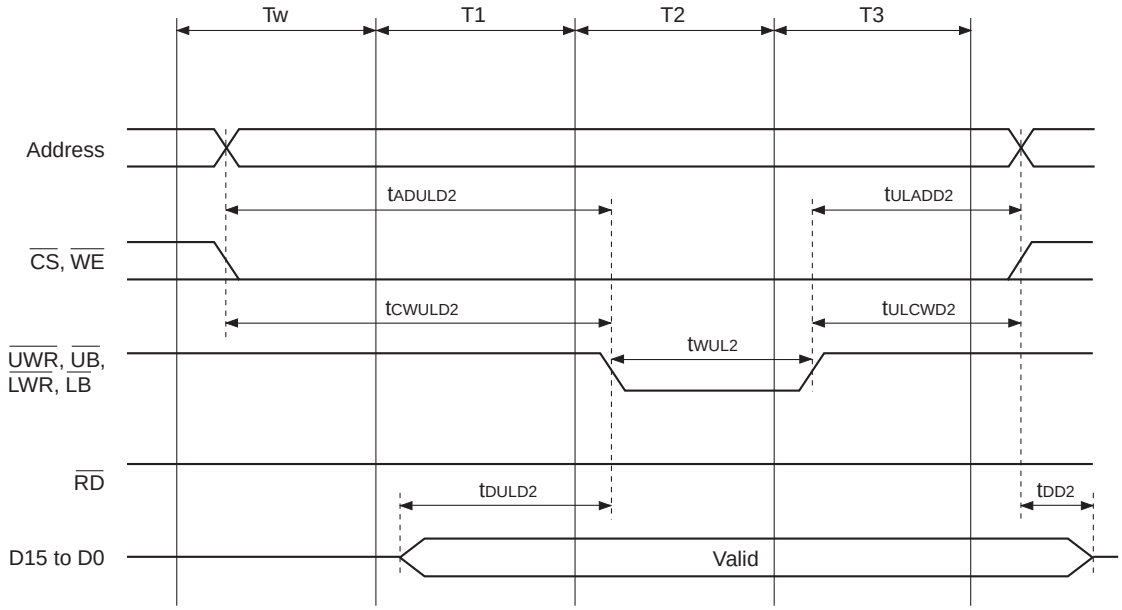


Fig. 7. 3-cycle Access Basic Timing in Write Operation

• 2-cycle access AC characteristics parameter in read operation

(Topr = –20 to +70°C, DV_{DD} = 1.1 to 1.3V, VDIO = 2.7 to 3.3V, DV_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit
Address, $\overline{CS}$ and $\overline{WE}$ setup time for $\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) ↓	t_{ADULD3}	$1/2f_{SRC}$ – 5	—	ns
$\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) low pulse width	t_{WUL3}	$1/f_{SRC}$	—	ns
Address, $\overline{CS}$ and $\overline{WE}$ hold time for $\overline{UWR}$ ($\overline{UB}$), $\overline{LWR}$ ($\overline{LB}$) ↓ and $\overline{RD}$↓	t_{ULADD3}	$1/2f_{SRC}$ – 5	—	ns
Data setup time for $\overline{UWR}$ ($\overline{UB}$), $\overline{LWR}$ ($\overline{LB}$) ↑ and $\overline{RD}$↑	t_{RDS1}	$1/2f_{SRC}$ + 23	—	ns
Data hold time for $\overline{UWR}$ ($\overline{UB}$), $\overline{LWR}$ ($\overline{LB}$) ↑ and $\overline{RD}$↑	t_{RDH1}	0	—	ns

Note) The load capacitance of the measurement pin is 75pF.

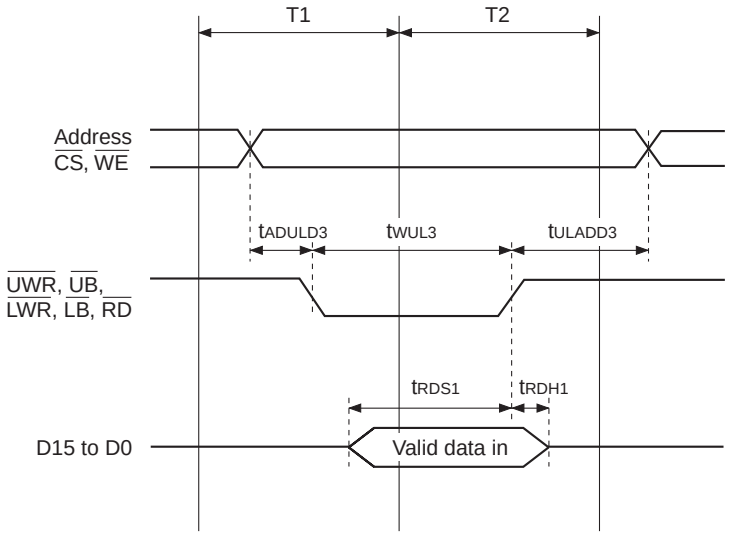


Fig. 8. 2-cycle Access Basic Timing in Read Operation

• 3-cycle access AC characteristics parameter in read operation

(Topr = –20 to +70°C, DV_{DD} = 1.1 to 1.3V, VDIO = 2.7 to 3.3V, DV_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit
Address, $\overline{CS}$ and $\overline{WE}$ setup time for $\overline{UWR}$ ($\overline{UB}$), $\overline{LWR}$ ($\overline{LB}$) ↓ and $\overline{RD}$↓	t_{ADULD4}	$1/f_{SRC}$ – 5	—	ns
$\overline{UWR}$ ($\overline{UB}$) and $\overline{LWR}$ ($\overline{LB}$) low pulse width	t_{WUL4}	$1/f_{SRC}$	—	ns
Address, $\overline{CS}$ and $\overline{WE}$ hold time for $\overline{UWR}$ ($\overline{UB}$), $\overline{LWR}$ ($\overline{LB}$) ↓ and $\overline{RD}$↓	t_{ULADD4}	$1/f_{SRC}$ – 5	—	ns
Data setup time for $\overline{UWR}$ ($\overline{UB}$), $\overline{LWR}$ ($\overline{LB}$) ↑ and $\overline{RD}$↑	t_{RDS2}	24	—	ns
Data hold time for $\overline{UWR}$ ($\overline{UB}$), $\overline{LWR}$ ($\overline{LB}$) ↑ and $\overline{RD}$↑	t_{RDH2}	0	—	ns

Note) The load capacitance of the measurement pin is 75pF.

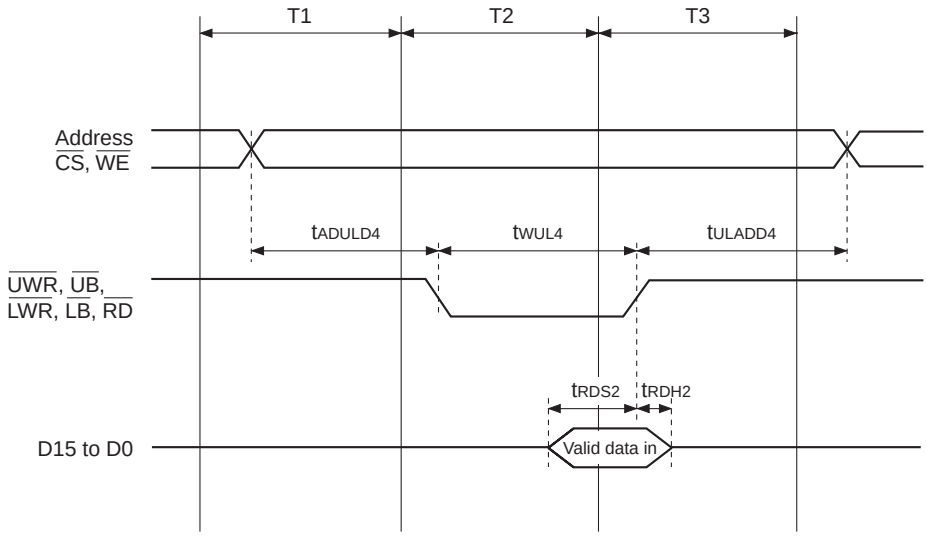


Fig. 9. 3-cycle Access Basic Timing in Read Operation

7) A/D converter characteristics

(Topr = –20 to +70°C, DV_{DD} = 1.1 to 1.3V, AVDAD = 2.2 to 3.0V, DVss = 0V, AVSAD = 0V reference)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit
Resolution		—	—	—	10	Bits
Absolute error		—	—	—	±7	LSB
Differential linearity error		—	—	—	±1	LSB
Integral linearity error		—	—	—	±3	LSB
Conversion time	t_{CONV}	—	$19/f_{PS4}$	—	$20/f_{PS4}$	µs
Sampling time	t_{SAMP}	—	—	$3/f_{PS4}$	—	µs
Analog input voltage	V_{IAN}	AN0 to AN7	0	—	AVDAD	V

Note) f_{PS4} is $f_{SRC}/16$ [MHz] relative to the main oscillation circuit output f_{SRC}.
Conversion time indicates the time required from the start of conversion when one channel is selected until the ADC interrupt request is generated, and also includes the sampling time.

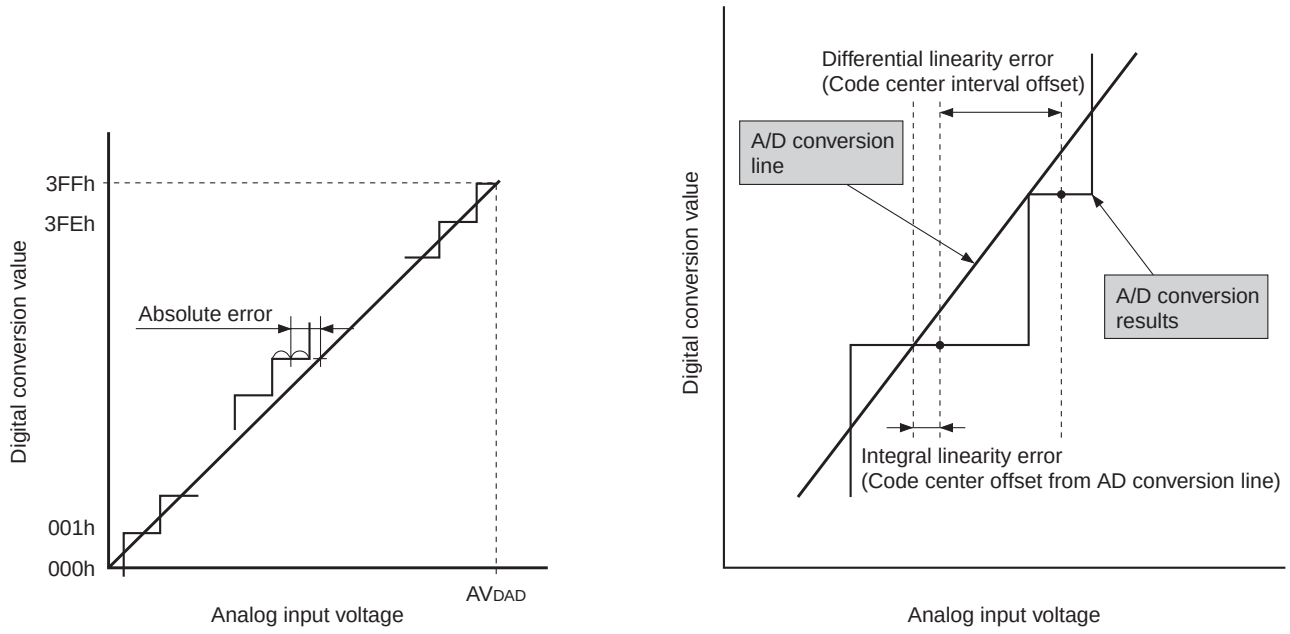


Fig. 10. Definition of A/D Converter Terms

Internal DAC Specifications

1) Digital filter characteristics

Pass band	0 [Hz] to 20 [kHz]
Stop band	24.1 to 328.7 [kHz]
Pass band ripple	±0.03 [dB] or less
Stop band attenuation	54 [dB] or more

2) Analog characteristics

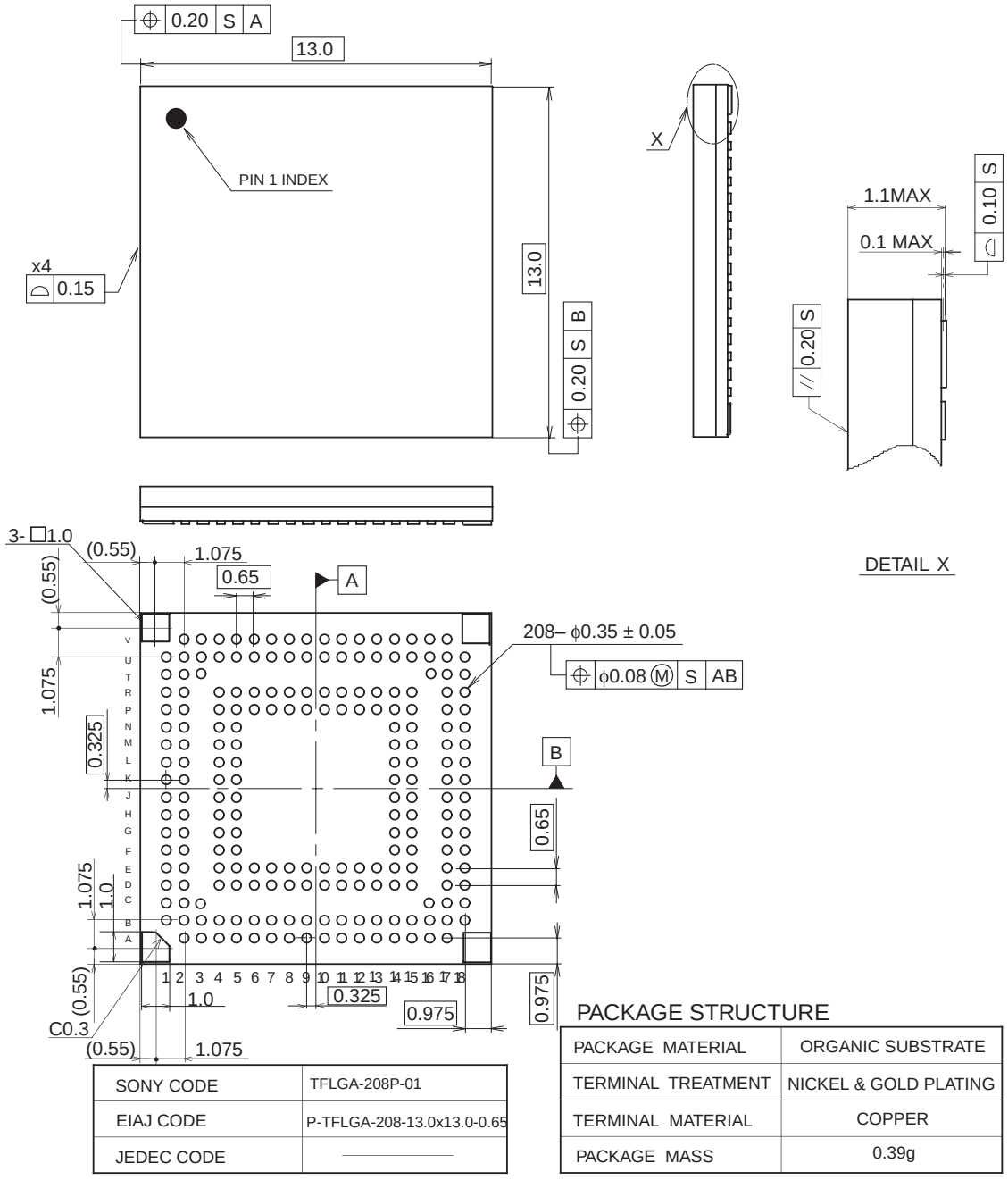
(AVDDA = 2.4V, Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
S/N	—	92	—	dB
THD + N	—	0.015	—	%
Dynamic range	—	93	—	dB
Gain difference between channels	—	0.1	0.15	dB or less
Output voltage*1	—	666.2	—	Vrms
Output load resistor	10	—	—	kΩ or more
Analog filter cutoff frequency	—	90	—	kHz

*1 The output voltage is approximately 0.8AVDDA [Vp-p].

Package Outline Unit: mm

208PIN TFLGA



SONY CODE	TFLGA-208P-01
EIAJ CODE	P-TFLGA-208-13.0x13.0-0.65
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	NICKEL & GOLD PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.39g